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Solid-State Electronics 47 (2003) 811–814
SOLID-STATE ELECTRONICS
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Fabrication and characteristics of polymeric thin-film capacitor

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Received 27 July 2002; received in revised form 2 September 2002; accepted 10 September 2002

Abstract

Polymer materials are attracting more and more attentions for applications to microelectronic devices due to their flexibility, lightweight, and low cost. In this paper, fabrication and characteristics of an all-polymer capacitor, using polypyrrole and poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) as a semiconductor and a gate layer, are reported. Dielectric polymer, polyvinylphenol, was applied as the insulator to the device. The all-polymer capacitor analogous to metal oxide semiconductor (MOS) device was fabricated by the conventional UV lithography techniques. The fabricated device was measured and characterized electrically. The results are compared with the electrical behavior of analogous silicon-based MOS devices. It demonstrates that the device operates in a very similar fashion to its conventional counterparts.

1. Introduction

Synthetic materials have existed for a whole century. Polymers have been used as packaging, and from anti-corrosion materials to smart materials. The most important development in the polymer world was the discovery of conducting polymers. It stimulated the polymer research on microelectronic applications.

Since the first polymer-based transistor with polyacetylene as the active semiconductor was fabricated by Ebisawa et al. in 1983 [1], lots of research work has been done in the field of organic devices. In 1989, the first polymer light emitting diode (LED) with polyphenylene–vinylene as the emissive layer was made by the University of Cambridge. In 1997, the first printed transistor in the world was developed at Lucent Technologies' research company, Bell Labs Innovations. Furthermore, the first all-polymer transistor by ink-jet printing technique was fabricated by Kawase et al. [2].

Ink-jet printing, lithography, thermal evaporation, reactive ion etching (RIE), hot embossing, self-assembly, and polymerization are the main technologies to fabricate polymer devices. The possibility of processing electrically conducting polymers by various coating techniques has enabled researchers to fabricate various electronic devices such as thin-film transistors, diodes, LEDs, capacitors, organic integrated circuits, organic wires, and electro-luminescent devices [3–8]. Polymer thin films can be coated on substrates such as glass, plastic, silicon, wood, or paper.

Except for the applications to microelectronics, polymers can also be applied to sensors, actuators [9–12], artificial muscles, and electrically conducting textiles, etc. [13].

There are rare reports about all-polymer devices fabricated by UV lithographic techniques, especially for all-polymer thin-film capacitors. In this paper, an all-polymer capacitor fabricated by UV lithography was presented in detail. Based on the testing results, the polymer metal oxide semiconductor (MOS)-like thin-film capacitor and the characteristics of conducting polymers were analyzed. At the meantime, the properties of the interface between different polymer materials were also investigated.

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PII: S0038-1101(02)00392-1

2. Experiments

The thin-film capacitor was fabricated by UV lithographic techniques. The device was made through the process outlined in Fig. 1(a)–(e). MOS-like structure was adopted, including three different polymer materials. P-type semiconducting polymer, polypyrrole (PPy), was used as the semiconductor. Conducting polymer, poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT/PSS) (Baytron P from Bayer AG), was applied as the gate material. The dielectric layer was PVP insulation polymer. All three polymers are solution-based and suitable for spin-coating. Fig. 1 illustrates the outline of the capacitor fabrication procedures.

A silicon wafer with a layer of silicon dioxide was used as the substrate. Three layers of polymers, PPy, PVP and PEDOT/PSS from the bottom to the top, were spun on the wafer respectively. Each layer was baked at 100–105 °C for 1–5 min before the next layer was spun. Then aluminum was deposited on top of the PEDOT/PSS by thermal evaporation. Aluminum, instead of photoresist (PR), was used as an etching mask because PR is difficult to remove selectively. Moreover, it was found that PVP can be dissolved in many organic solvents such as AZ300 (PR 1813 developer), ethyl alcohol, and isopropyl alcohol, etc. Even PR itself can dissolve PVP to some degree. Aluminum was also used to prevent polymer layers from being attached during the UV lithography. Finally the polymer capacitor was patterned with dry etching. Two minutes RIE was enough to remove the PEDOT/PSS and PVP layers.

Though only basic lithographic techniques applied, several issues need to be considered and avoided. Moisture inside the polymer layers can cause the polymer degradation. One method to solve this problem is to bake each layer dry completely after spin-coating step. The other way is to make the fabrication process continuously to prevent moisture from being introduced. Moreover, the device also needs to be baked after longer period time between two fabrication steps.

Spin-coating is the main fabrication approach. There are several advantages of spin-coating, such as fine structures and global planarization. However, problems still exist and affect the performance of the electronics devices. For example, gap-filling, multilevel structures and shrinkage may be introduced by spin-coating. The other issue related to the multilayer spin-coating is the interlayer mixing, occurring at the interface between two layers. It is due to the penetration of the solvents of the later spin-coating polymer into the previous polymer film. The function of the interlayer mixing can assist or confine the carrier transport between the two layers. Proper control of film morphology resulting from the polymer deposition process remains a challenge [14]. It is certain that some of the mentioned issues have involved in the fabrication process and affect the electrical properties of the thin-film capacitor.

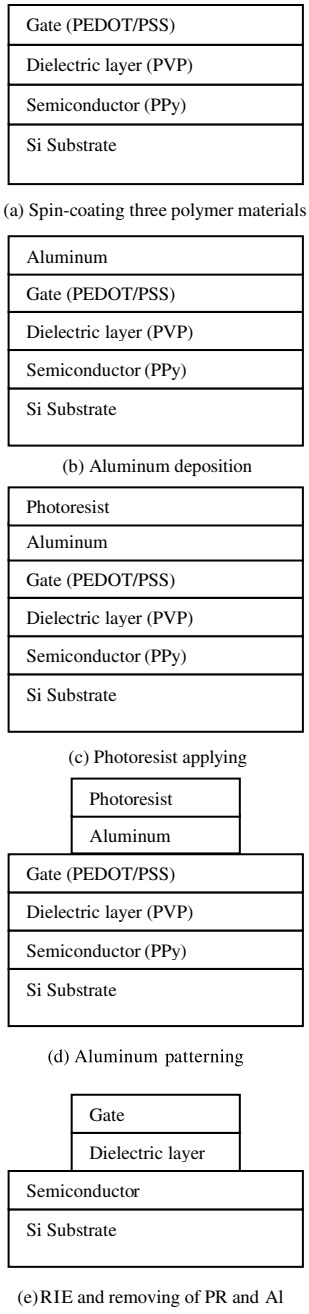

Fig. 1. Outline of the thin-film capacitor fabrication process.

3. Electrical properties

The thin-film capacitor was characterized in air with Keithley Test and Measurement Instrument. Keithley

software provides comprehensive analysis to the measured and calculated parameters. There are two models for testing quasistatic and high frequency capacitance in the System 82 simultaneous C–V System with windows-based Metrics-ICS C–V software. Figs. 2 and 3 show the electrical characteristics of the capacitor.

In Fig. 2, the curve of quasistatic capacitance of the polymer capacitor is similar to that of a conventional silicon-based capacitor. The accumulation, depletion and inversion modes in the capacitor can be demonstrated through the capacitance–voltage relationship. The capacitance is given by the series capacitance of the insulator layer (C_i) and the depletion layer (C_d), and is given by

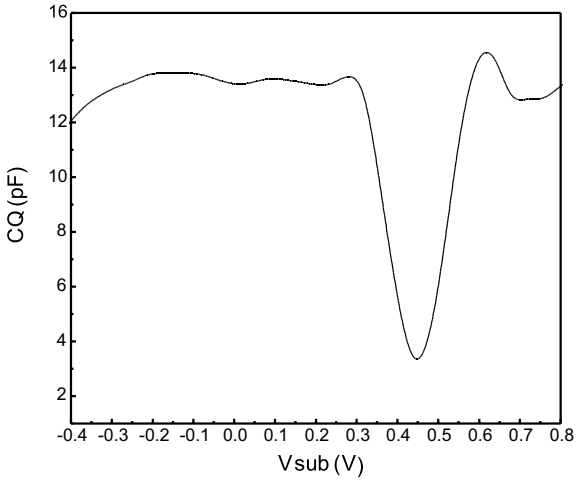

Fig. 2. Quasistatic capacitance curve of the all-polymer capacitor.

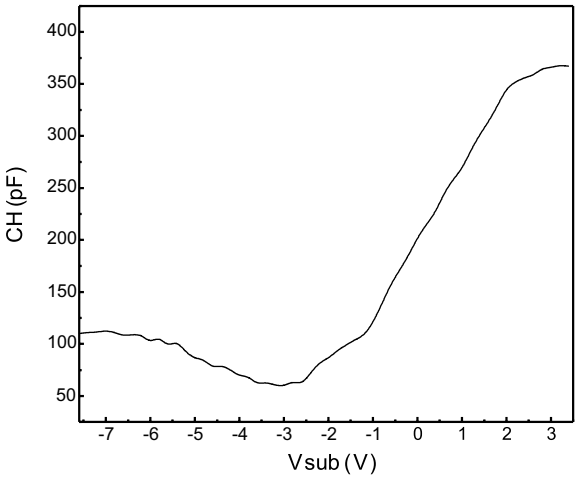

Fig. 3. High frequency capacitance curve of the all-polymer capacitor.

$$C = C_i C_d/(C_i + C_d)$$

The formation of the accumulation layer for negative bias voltage is illustrated in Fig. 2, as the tested capacitance tends towards the capacitance of the insulating layer. The capacitance decreases as the bias voltage becomes more positive, showing the formation of the depletion layer. Inversion is caused by the accumulation of the minority carriers beneath the insulator. The production of minority charge carriers is controlled by the thermal generation rate of electro-hole pairs [15], a relative slow process. In order to obtain the onset of the inversion, the testing parameters need to be adjusted carefully to make the minority carriers capable to follow the probe signal and accumulate under the insulator.

It was found that swelling occurs during the spin-coating PVP dielectric film. It caused the capacitance value unstable due to the non-uniform thickness of the film. To solve this problem, one method is to change the insulation material, and another one is to adopt gas phase deposition, such as thermally evaporating the PVP powder.

For understanding the high frequency capacitance shown in Fig. 3, charge storage is the key factor to explain it. Unlike the conventional charge storage in semiconductors, charges injected into the valence and conduction bands are not expected to remain in the band states. The structural relaxation around the charges occurs when charges are added to the polymer chains. The processing of conducting polymers degenerate ground state with a preferred sense of bond alternation, and the localized states are the bond alternation defects known as solitions [15]. The formation of solitions in conducting polymers may be shown by the appearance of new optical absorption below the bandgap associated with the solution vibrational and electronic transitions [13]. The capacitance is the change in charge density at interface between the insulator and the conducting polymer, and these added charges are stored in solution-like states, and then $\partial Q/\partial V$ can represent the capacitance.

The whole structure of the capacitor consists of three layers of polymers and two polymeric interfaces. The top and bottom layers are the electrically conductible polymers. For the PEDOT/PSS, it works as the conducting polymer. However, the dopant concentration of the PEDOT/PSS is about 10^{20} cm^{-3}. Strictly speaking, it is a heavily doped semiconductor. With extra bias voltages applied onto the device, the charges will be accumulated or depleted at the interfaces. The rate of holes accumulation at the PEDOT/PSS-PVP interface is faster than the rate of holes depletion from the PVP–PPy interface. It results in $\partial Q/\partial V$ increasing as more positive bias voltages applied. Further increasing positive voltage, the accumulation rate and the depletion rate reach the dynamic balance, and the capacitance increases

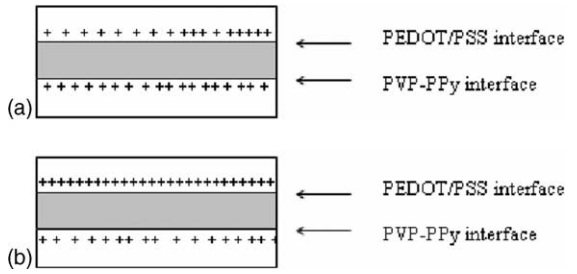

Fig. 4. Charge transportation at the interfaces of the thin-film capacitor. (a) At the beginning of bias voltage; (b) increasing positive bias voltage.

slowly. Finally the saturation of the capacitance for large positive voltage is due to the depletion layer extending completely across the conducting polymer films. Fig. 4 shows the charge transportation at the interfaces when applying bias voltages.

At high frequencies, as the minority carriers are unable to follow the extra signal, a deep depletion capacitance may exist. It maybe resulted from the ''quickly'' sweeping gate voltage. ''Quickly'' means that the gate voltage must be changed fast enough so that the structure is not in thermal equilibrium. It causes a wider depletion region compared to the silicon-based counterparts.

4. Conclusions

An all-polymer MOS-like capacitor fabricated by UV lithographic technique was realized successfully. The conducting polymer as an active semiconducting component in this microelectronic device behaved in the similar fashion as the silicon-based counterpart at accumulation, depletion, and inversion regions. UV lithographic technique is a simple and convenient approach to fabricate polymer-based microelectronic devices. There are still some problems and open questions for further investigation and testimony. Though polymer fabrication is an immature technology, polymeric devices or systems will have huge potential applications to microelectronics, optoelectronics and MEMS.

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