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Thin-film transistors with controllable mobilities based on layer-by-layer self-assembled carbon nanotube composites

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ABSTRACT

We report thin-film transistors (TFTs) capable of controlling mobilities in a broad range using self-assembled nanocomposite multilayers. Single-walled carbon nanotubes (SWNTs) and SiO_2 nanoparticles are vertically stacked on a substrate as the semiconducting and dielectric materials, respectively. The number of assembled layers can adjust the nanotube interconnection and tune the mobilities of the transistors. Our experiments show that the mobility can be enhanced to 35 times, and the highest observed mobility is 333.04 cm^2/V s. Furthermore, we find that the reliability of the devices is increased with the increasing number of SWNT layers in the film. Our results demonstrate an effective technique to produce reliable and high-performance thin-film micro/nanoelectronic devices.

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1. Introduction

Mobility is one of the most important parameters of transistors. It represents the charge drift velocity in the conductive channel of the device. Researchers have discovered several approaches to control the mobility. For traditional silicon field-effect transistors (FETs), the controllability is mainly achieved by the impurity doping methods. However, the mobility is limited by the scattering effect, and the range of the change is less than 15 [1]. For organic FETs, growing a self-assembled monolayer (SAM) between the semiconducting and the dielectric layers can change the charge density and the mobility of the device [2]. Other reported approaches include modifying the semiconducting channel thickness [3], adjusting the deposition parameters [4], and tuning the molecular order of the film [5]. However, many of these reported FETs suffer from low mobilities, 0.01–10 cm^2/V s, and limited mobility tuning factors, 5–20.

Single-walled carbon nanotubes (SWNTs) are considered to be one of the ideal candidates for next-generation electronic devices [6]. At room temperature, the intrinsic mobility of an individual semiconducting SWNT can exceed 100,000 cm^2/V s, higher than any other known semiconductors [7]. Individual SWNT transistors show high carrier mobility of 3000 cm^2/V s [8]. However, the throughput of these devices is limited due to the complicated fabrication processes. In contrast, SWNT thin-film transistors (TFTs) are easier to produce, and have a higher yield. Even though the mobility is relatively low, normally in the range of 1–150 cm^2/V s, SWNT TFTs still have attracted considerable attention recently [9]. The reported SWNT thin films are mostly monolayers, in the form of aligned arrays or random networks.

Here we report a multilayer design of SWNT TFTs. Compared with most monolayer TFTs, the semiconducting channels are composed of SWNT multilayers: the layers are deposited on the substrate in a repeated fashion with polyelectrolytes as the intermediate adhesion material. Highly ordered "sandwich" multilayer structures are constructed based on the electrostatic force between oppositely charged components. The stacked SWNT multilayer is used as the semiconducting film for the TFT. The degree of nanotube interconnections is highly affected by the number of assembled layers so that the conductivity and the carrier mobility of the TFT can be adjusted.

2. Design and fabrication of thin-film transistors

Layer-by-layer self-assembly is a solution-based process, and the pristine SWNTs need to be treated with acids to increase the solubility in water, as described elsewhere [10]. The SWNT TFT is

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based on our previously reported devices [11]. The transistors are fabricated on Si/SiO_2 wafers with self-assembled SWNTs as the semiconducting material, SiO_2 nanoparticles as the gate dielectric material, Au as the source and drain electrode material, and Al as the gate electrode material. The device structure and the assembled nanotube/nanoparticle multilayers are illustrated in Fig. 1.

The fabrication combines the "top-down" lithography and the "bottom-up" layer-by-layer self-assembly techniques, as shown in Fig. 2. First, Cr/Au (100/200 nm) metal layers are evaporated on the substrate, and patterned as source (S) and drain (D) electrodes. Second, a layer of photoresist is spin coated on the substrate and patterned as the sacrificial structures. Third, SWNT and SiO_2 multilayers are self-assembled on the substrate as the semiconducting and insulating layers, respectively. Fourth, a layer of Al 110 nm thick is evaporated on the wafer surface as the top gate (G) electrode. The last step is to soak the whole wafer in acetone for 2 min. This lift-off process removes the photoresist sacrificial layer and other layers on top. After this step, only the multilayers directly coated on the substrate remain on the surface.

Fig. 3 shows the scanning electron microscope (SEM, JEOL 6500) images of the device and the coated multilayers. The three electrodes are elongated for easy probing and characterization. The randomly assembled SWNTs and polyelectrolytes form a strong and uniform composite film. The SiO_2 nanoparticles (45 nm in diameter) are closely packed. The cross-sectional SEM image shows the sidewall of the film, which contains the vertically stacked SWNT and SiO_2 nanoparticle multilayers. The unique feature of the SWNT TFTs is that the film thickness is directly controlled by the number of assembled layers. With the positively charged polyelectrolytes, poly(dimethyldiallylammonium chloride) (PDDA), as the electrostatic "glue", the negatively charged SWNTs and SiO_2 nanoparticles can be easily deposited on the substrate. In the experiments, we fix the thickness of the dielectric film as a constant, and only adjust the thickness of the semiconducting film. The thickness of a (PDDA/SWNT) bilayer is 7.6 nm [12]. A multilayer with six SiO_2 nanoparticle layers serves as the dielectric film, and the effective thickness is 180 nm. Both values are obtained with a quartz crystal microbalance (QCM, QCM, Maxtek RQCM). The deposition of SiO_2 nanoparticle layers is further discussed below. Fig. 4 shows the three-dimensional (3D) surface profile of a SWNT TFT obtained by an optical profiler (Wyko NT1100).

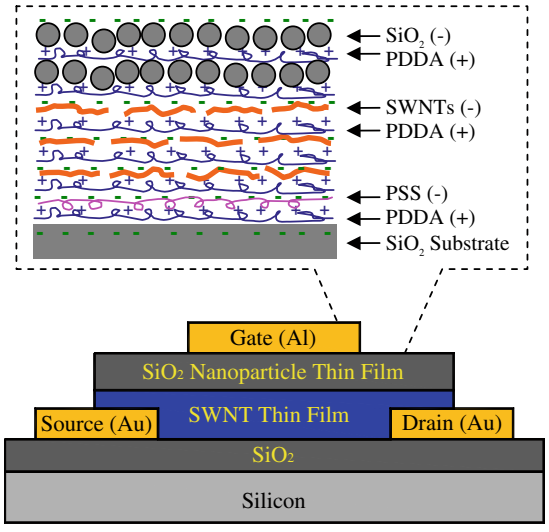

Fig. 1. Structure of the carbon nanotube thin-film transistor. The enlarged part shows the layer-by-layer self-assembled carbon nanotube semiconducting layer and SiO_2 nanoparticle dielectric layer.

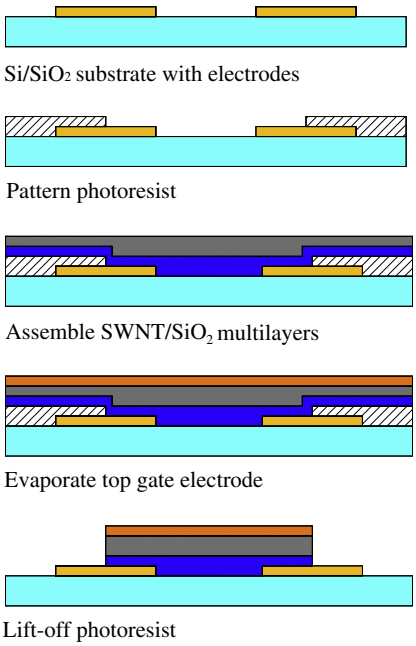

Fig. 2. Schematic process flow of the carbon nanotube thin-film transistor.

3. Characterization of thin-film transistors

The fabricated SWNT TFTs are characterized using a semiconductor parameter analyzer (HP 4156A). All measurements are carried out in an ambient environment at room temperature. The characteristics of two SWNT TFTs are shown in Fig. 5. The channel width W and length L of the devices are 500 and 25 μm, respectively. Both devices show typical p-channel transistor behavior with holes as the majority carriers. They operate in an accumulation mode with a negative drain voltage V_D and a negative gate voltage V_G. The negative V_G attracts holes to the top surface of the semiconducting film. Consequently, the accumulated holes increase the surface conductivity and create a conductive channel below the SWNT-SiO_2 interface. The number of the accumulated holes and the surface conductivity are proportional to V_G. The first TFT has only one assembled SWNT layer in the semiconducting channel. The drain current $|I_D|$ increases with $|V_G|$, and it is in the μA range, e.g., $I_D = -70$ μA at $V_D = -5$ V and $V_G = -10$ V (Fig. 5a). Fig. 5b illustrates the gate transfer characteristics of the same device. The device operates at the saturation region with $V_D = -5$ V. A threshold voltage $V_{th} = -2.3$ V is obtained by linearly extrapolating the gate transfer curve $(-I_D)^{1/2}$–V_G to the x-axis. To estimate the carrier mobility, the device is analyzed using the standard metal-oxide-semiconductor field-effect transistor (MOSFET) equation [1]

$$I_D(saturation) = \frac{WC_i\mu_p}{2L}(V_G - V_{th})^2 \quad (1)$$

where $I_D(saturation)$ is the measured drain current at the saturation region, $W = 500$ μm and $L = 25$ μm are design parameters, V_G is a controlled signal, V_{th} is obtained from the transfer characteristics, and C_i is the capacitance per unit area of the gate insulating layer. Therefore, the hole mobility μ_p in the semiconducting layer can be calculated by

$$\mu_p = \frac{2LI_D(saturation)}{WC_i(V_G - V_{th})^2} \quad (2)$$

$$C_i = \frac{\varepsilon_0\varepsilon_r}{d} \quad (3)$$

where $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm is the permittivity of free space, ε_r is the relative dielectric constant, and d is the thickness of the dielec-

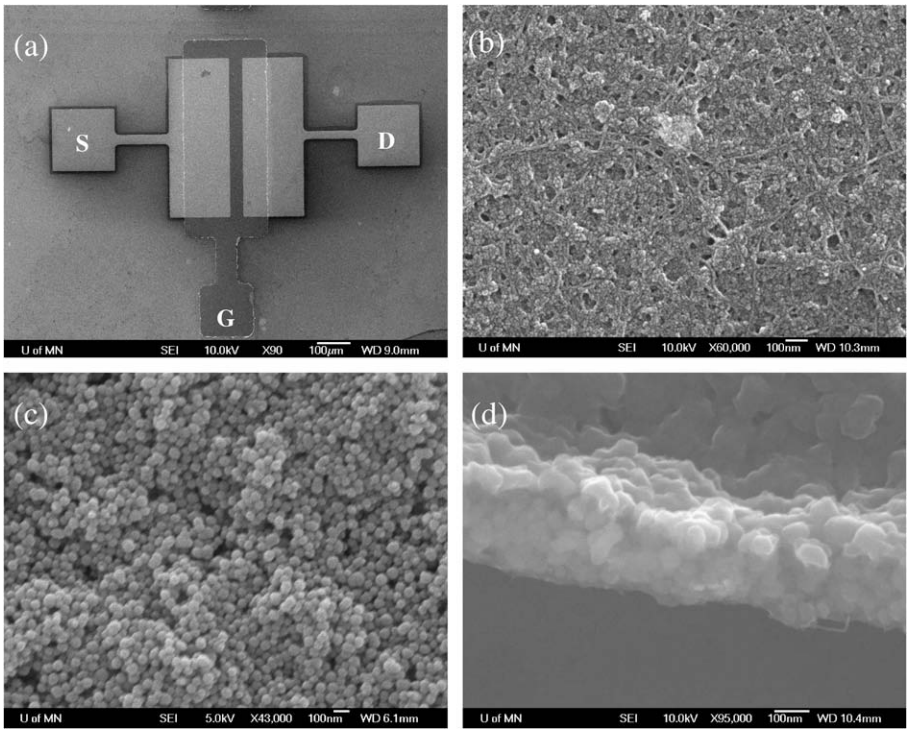

Fig. 3. Scanning electron microscope (SEM) images of (a) a fabricated SWNT TFT, self-assembled (b) SWNTs and (c) SiO_2 nanoparticles. (d) Cross-sectional SEM image of the assembled multilayers. The device used for the SEM inspection consists of five SWNT layers and six SiO_2 nanoparticle layers.

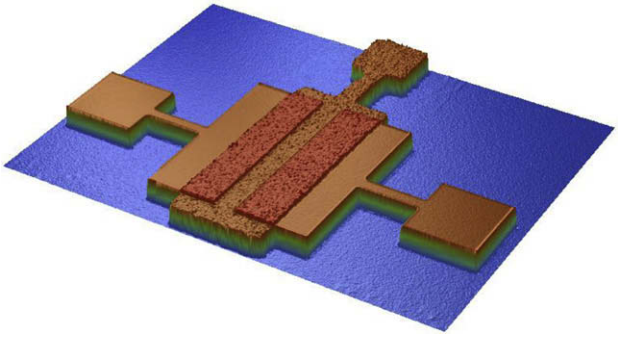

Fig. 4. 3D surface profile of a thin-film transistor obtained by an optical profiler.

tric layer. As investigated by Hua et al., the relative dielectric constant of the SiO_2 nanoparticle film formed by the layer-by-layer self-assembly method is 6 [13], higher than that of the thermal oxide (3.9). The higher dielectric constant increases the gate capacitance and facilitates the hole accumulation in the channel.

The thickness of the assembled SiO_2 nanoparticle layer is characterized by a QCM. An AT-cut, 9 MHz, 1 inch diameter quartz crystal with Au electrodes is used as the sensing device. The frequency shift of the crystal represents the coating of the nanoparticles on the Au surface and can be further converted to film thickness based on the Sauerbrey equation [14]. The QCM characterization shows that the effective thickness of a (PDDA/SiO_2) bilayer is approximately 30 nm, similar to the value reported earlier by Cui et al. [15] The apparent difference between the effective thickness of the film and the diameter (45 nm) of SiO_2 nanoparticles comes from the air-filled pores in the multilayer. As investigated by Lvov et al., the volume ratio of the SiO_2 nanoparticles in a layer-by-layer self-assembled multilayer is approximately 60%, which is close to the theoretical dense-packing coefficient for spheres (63%); and the volume composition of the film is: 60% SiO_2 + 10% PDDA + 30% pores [16]. Given the dielectric films for all devices contain six (PDDA/SiO_2) bilayers, the thickness is calculated as 180 nm. Combining all the factors, the dielectric capacitance per unit area can be calculated as $C_i = 2.95 \times 10^{-8}$ F/cm^2 from Eq. (3).

The hole mobility of this device $\mu_p = 3.31$ cm^2/V s can therefore be obtained by substituting C_i into Eq. (2). Other key parameters of this device are calculated as: on/off ratio $I_{on/off} = 14.3$ and normalized transconductance $g_m/W = (dI_D/dV_G)/W = 0.023$ S/m.

The characteristics of a similar TFT are shown in Fig. 5c and d. This transistor has the same structures and dimensions as the first one. The only difference is that its semiconducting film consists of three SWNT layers. The key parameters of this device are: $V_{th} = -2$ V, $\mu_p = 116.31$ cm^2/V s, $I_{on/off} = 5.01$, and $g_m/W = 0.82$ S/m. Compared with the one-SWNT-layer transistor, this device shows an obvious current increase: $I_D = -2.59$ mA at $V_D = -5$ V and $V_G = -10$ V.

However, leakage current from the source to the gate can be observed. For the two devices characterized in Fig. 5, the maximum leakage currents are 696 nA (for the one-SWNT-layer device) and 4.2 μA (for the three-SWNT-layer device), respectively. The leakage currents are considerably small: less than 1% of the total current measured at the drain electrode. However, they can cause problems in device operation and increase the power consumption of the device. Further investigation will be conducted to reduce the leakage current. One potential solution is to use plasma-enhanced chemical vapor deposition (PECVD) method to coat the gate oxide. The PECVD technique can grow a denser dielectric film and reduce the leakage current.

To obtain a better understanding of the multilayers and the transistors, we fabricate and measure a group of devices with various numbers, from 1 to 7, of SWNT layers. Other parameters of the fabrication process and the device structures are kept the same. The devices are divided into seven groups based on n, the number of SWNT layers. We arbitrarily choose five devices from each group for characterization. If one device demonstrates explicit field effect

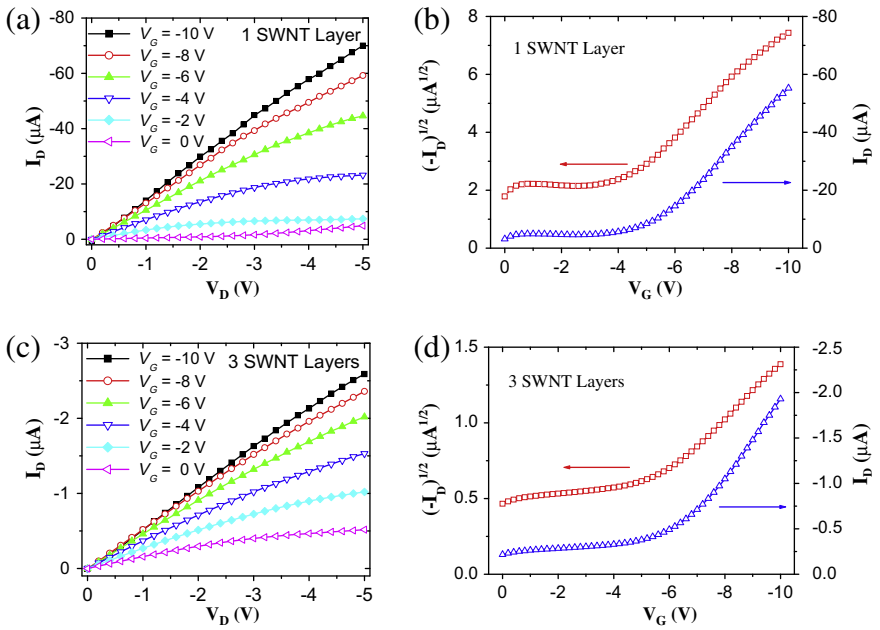

Fig. 5. (a) Output and (b) transfer characteristics of a SWNT TFT with one assembled SWNT layer. (c) Output and (d) transfer characteristics of a similar device with three assembled SWNT layers.

in the I_D–V_D curves, it is considered functional and the key parameters are calculated accordingly. Fig. 6 (main panel) shows the experimental results for a set of SWNT TFTs with channel dimensions of $W = 500$ μm and $L = 25$ μm. The solid squares represent the average mobilities of the functional devices, and the error bars indicate the standard deviation. A steep mobility increase can be seen when n increases from 1 to 3; i.e., the mobility is increased 34.9 times in this region. Afterwards, the mobility slowly decreases to 96.51 cm^2/V s where $n = 7$. Another set of transistors with $W = 500$ μm and $L = 50$ μm is also characterized for verification, as shown in Fig. 6 (inset). These devices show a similar behavior: the mobility greatly increases first, and slowly decreases to a smaller value afterwards. The average mobilities for devices with $n = 1$, 3, 7 are measured as 6.52, 244.77, and 99.29 cm^2/V s, respectively. One transistor with $n = 4$, $W = 500$ μm, and $L = 50$ μm demonstrates a high mobility of 333.04 cm^2/V s.

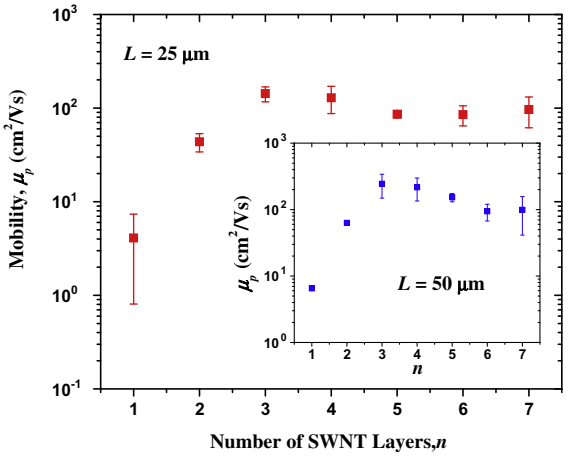

Fig. 6. Mobility of SWNT TFTs with various numbers of SWNT layers (n: 1–7). Main panel, experimental results for devices with $W = 500$ μm and $L = 25$ μm. Inset, mobility versus n for devices with $W = 500$ μm and $L = 50$ μm.

The dependence of the mobility on the number of SWNT layers, n, is probably due to the interconnections among the SWNTs. There are two types of interconnections: one occurs among SWNTs in the same layer and the other one occurs among SWNTs from different layers. The SWNT network in a single layer is sufficient to establish a conductive channel for the carrier transfer. The typical mobility range of our SWNT monolayer transistors is 1–10 cm^2/V s, very close to other reported monolayer devices [17,18]. For the multilayer, the SWNT layers are "glued" together by the intermediate polyelectrolyte layers. Similar to the SWNTs, the polyelectrolytes have long chain structures. Even after saturated adsorption, it is still difficult for the polyelectrolytes to completely separate the adjacent SWNT layers. The SWNTs from one layer can penetrate through the polyelectrolyte layers, and connect to the SWNTs from other layers. The interconnection among the SWNTs increases the effective thickness of the semiconducting film and the mobility of the conductive channel. A similar result was observed for SWNT multilayers assembled on flexible substrates in an earlier investigation [19].

After the number increases to 3, the mobility of the TFTs becomes relatively stable with a slight decrease. The reason of this behavior is not fully understood at present. One possibility is the presence of the polyelectrolytes and the air-filled pores in the multilayers. The dielectric constant of the polyelectrolytes is in a range of 30–120 [20]. As the number grows, on the one hand, the better interconnection among the SWNTs increases the conductance of the semiconducting film; on the other hand, however, the increased number of polyelectrolytes and the air-filled pores decreases its conductance. These two factors likely counterbalance each other, and may result in a stable mobility of the transistor. Furthermore, in the self-assembly process, the SWNT layers are deposited in a repeated fashion. The (PDDA/SWNT) bilayers are parallel to each other and they are all connected to the electrodes. Because of the high dielectric constant of PDDA, each SWNT layer can be considered as a resistor in a parallel circuit [19]. As the number of layers increases, the effect from each layer becomes less important.

In contrast to the aligned arrays, SWNT random networks cannot always guarantee the continuity of the films. Although the

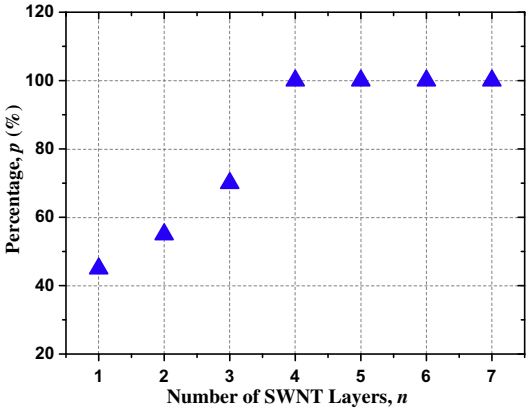

Fig. 7. Percentage of the functional devices p versus n.

deposited SWNTs can be densely packed in some areas, they can be sparsely packed in other areas. This uncertainty problem can be easily solved by the layer-by-layer self-assembled films. We study the reliability and stability of the SWNT TFTs by checking the percentage of the functional devices (Fig. 7). Again, we divide the transistors into seven groups depending on the number of layers, and choose 20 devices from each group. To enhance the sampling, we broaden the selection criteria and choose devices with various channel lengths: 5, 10, 25, and 50 μm. The 20 devices are divided into four sub-groups based on the channel length, and each subgroup has five devices. The sampling of the devices in the subgroups is arbitrary. In our measurement, all the devices are functional when the number of layers is more than 4. Clearly, the multilayer films assure the interconnection among the SWNTs and the electrical continuity of the film.

Table 1 summarizes the key parameters of the SWNT TFTs. The threshold voltage shifts in the range of −1.25 to −3.33 V with no obvious trend. This shift is mainly caused by the deposition process in the liquid phase and the resulting film quality. Both active components of the SWNT TFTs, (PDDA/SWNTs) and (PDDA/SiO_2) multilayers, are composite films. During the deposition, the assembled materials may have different orientations and coat at different locations. As a result, the fabricated devices show differences in their performances and shifts in some parameters including the threshold voltage. The other major concern of the devices is the low on/off ratio. The acid treatment introduces covalently attached carboxylic groups to the pristine SWNTs. These groups not only increase the solubility of the SWNTs, but also likely change their electrical properties. The presence of metallic SWNTs, roughly 1/3 of the pristine material, is another reason for the high off-state current. The most effective method to increase the on/off ratio is a proper material selection. For example, double-walled carbon nanotubes (DWNTs) can reduce the material damage during the acid treatment. Only the outmost walls contain the functional groups, and the inner tubes remain almost unmodified. In addition, if the metallic tubes can be effectively eliminated and only the semiconducting tubes are used in the multilayer, we can reasonably expect to fabricate TFTs with a much lower off-state current and a much higher on/off ratio. Further investigation will be conducted to gain a more precise insight of this problem to enhance the on/off ratio of self-assembled SWNTs based TFTs.

Table 1
Summary of the characterization data of SWNT TFTs with W = 500 μm and L = 25 μm. The values are obtained by averaging the data of three to five devices.

n	μ_p (cm^2/V s)	V_{th} (V)	$I_{on/off}$	g_m/W (S/m)
1	4.09	−1.5	12.6	0.031
2	43.66	−2	4.18	0.37
3	142.63	−3.33	4.69	0.88
4	129.07	−2.3	2.52	1.18
5	86.01	−3	5.03	0.54
6	85.15	−1.13	2	0.84
7	96.51	−1.25	2.36	0.84

4. Conclusion

In conclusion, we have demonstrated SWNT TFTs with high and controllable mobilities compared to organic TFTs. The SWNT TFT demonstrates a mobility of 333.04 cm^2/V s. With the integrated micro/nanofabrication technique, we are able to control the shape and thickness of the SWNT multilayer films. This technique has a high potential in fast, low-cost, and mass device fabrication of thin-film electronics. The vertically stacked SWNT layers have direct influence on the performance of the transistors. Mobility enhancement as large as 35 times can be achieved. The reliability of the devices is greatly increased by increasing the number of assembled SWNT layers in the film. The results indicate that the SWNT TFTs using the self-assembled multilayers are promising candidates for high-performance thin-film electronics.

Acknowledgement

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