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Cite as: Appl. Phys. Lett. **89**, 163512 (2006); https://doi.org/10.1063/1.2361278
Submitted: 12 June 2006 . Accepted: 31 August 2006 . Published Online: 19 October 2006

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High-mobility transistors based on nanoassembled carbon nanotube semiconducting layer and SiO_2 nanoparticle dielectric layer

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(Received 12 June 2006; accepted 31 August 2006; published online 19 October 2006)

The authors report the fabrication and characterization of high-mobility thin-film transistors (TFTs) using layer-by-layer (LBL) nano self-assembled single-walled carbon nanotubes (SWCNTs) as the semiconducting material and SiO_2 nanoparticles as the gate dielectric material. The channel length and the effective thickness of the SWCNT semiconductor layer are 50 μm and 38 nm, respectively. The effective thickness of the SiO_2 dielectric layer is 180 nm. The SWCNT TFT exhibits *p*-type semiconductor characteristics and operates in the accumulation mode, with a hole mobility (μ_p) of 168.5 $cm^2/V\,s$, a normalized transconductance (g_m/W) of 0.5 S/m, a threshold voltage (V_{th}) of −3 V, and an on/off current ratio ($I_{on/off}$) of 4.2. The combination technique with LBL nano self-assembly and microlithography provides a simple, low-temperature, and highly efficient approach to fabricate inexpensive TFT devices. © *2006 American Institute of Physics*.
[DOI: 10.1063/1.2361278]

Single-walled carbon nanotube (SWCNT) devices have been developed due to the outstanding structural, mechanical, thermal, electrical, and chemical properties of SWCNTs. In the long term, nanoelectronic devices are considered to be one of the most valuable applications of SWCNTs. At room temperature, the intrinsic mobility of an individual semiconducting SWCNT can exceed 100 000 $cm^2/V\,s$, which is higher than any other known semiconducting materials.[1] Field-effect transistors (FETs) based on individual carbon nanotubes (CNTs) have been fabricated by researchers. Compared with traditional Si FETs (with intrinsic electron mobility of 1500 $cm^2/V\,s$ and hole mobility of 450 $cm^2/V\,s$),[2] the individual-CNT FETs show higher carrier mobility of 3000 $cm^2/V\,s$.[3,4] However, the complexity of the fabrication process prevents the commercialization of individual CNT-based FETs.

An alternative approach is to use SWCNT thin film, in the form of either aligned array[5] or random network,[6] as the semiconducting channel layer. SWCNT thin-film transistors (TFTs) have been developed and characterized. The SWCNTs in the thin film interconnect and form a path for charge carriers. Techniques to deposit SWCNT thin films include soaking the device in the SWCNT solution,[7] dropping the SWCNT suspension on the substrate,[8] and using chemical vapor deposition systems.[9] However, these processes are either time consuming (~50–100 h), lacking in accuracy, or based on complex systems. The carrier mobilities of these SWCNT TFTs are in the range of 1–150 $cm^2/V\,s$.

The layer-by-layer (LBL) nano self-assembly technique allows one to obtain ultrathin films with high controllability, reproducibility, reliability, and versatility. The vertical dimension of the thin films can be controlled in nanometer scale. LBL nano self-assembly technique has been investigated by several groups to deposit SWCNT thin films for various applications, such as ultrahard composite thin films,[10] amperometric choline biosensors,[11] biocompatible platform for neuroprosthetic implants,[12] etc. However, we have not been aware of the application of using LBL nano self-assembled SWCNT thin film as the semiconducting layer for field-effect transistor.

In this letter, we report the use of the simple, fast, low-cost, and low-temperature self-assembly technique to deposit SWCNT thin film on a silicon substrate as the semiconducting layer for TFT. The SiO_2 nanoparticle thin film is also self-assembled on the substrate as the gate dielectric layer. The TFT based on self-assembled SWCNT thin film is fabricated with lower cost and shorter processing time, but has higher mobility than other reported SWCNT TFTs.[5–9]

In previous reports, we demonstrated the lithographic approach to pattern LBL nano self-assembled nanoparticle thin films.[13] Using this approach, self-assembled nanoparticle-based TFTs were fabricated and characterized. SiO_2 nanoparticles were selected as the dielectric material. Both SnO_2 (Ref. 14) and In_2O_3 (Ref. 15) nanoparticles were selected as the semiconducting materials. However, the carrier mobilities of these TFTs are relatively low, only in the range of 10^{-3}–10^{-1} $cm^2/V\,s$. Therefore, SWCNT is selected as the semiconducting material due to its high intrinsic mobility and high carrier carrying capability.[10] The structure and the test scheme of the SWCNT TFT are illustrated in Fig. 1. SWCNT and SiO_2 nanoparticle thin films are the semiconducting and dielectric layers, respectively. Gold (Au) is used as the source and drain electrode material; aluminum (Al) is used as the gate electrode material.

In order to self-assemble SWCNT and nanoparticle thin films, several commercially available chemicals were used.

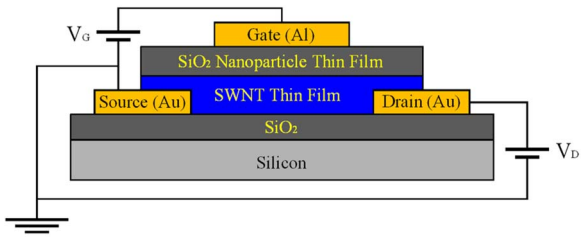

FIG. 1. (Color online) Structure and test scheme of a TFT fabricated with LBL nano self-assembly and microlithography.

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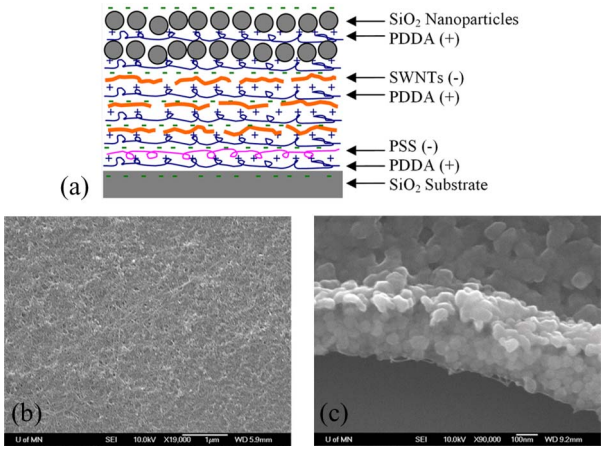

FIG. 2. (Color online) (a) Model structure of LBL self-assembled SWNCT semiconducting layer and SiO_2 nanoparticle dielectric layer. (b) SEM image of the assembled SWNCTs. (c) Cross-sectional SEM image of the assembled SWCNT/SiO_2 layers.

The concentrations of SiO_2 nanoparticle dispersion, PDDA, and PSS are 40, 15, and of 3 mg/ml, respectively. Pristine SWCNTs were treated with a mixture of nitric and sulfuric acids (1:3 HNO_3:H_2SO_4) at 110 °C for 45 min. This process increased the solubility of SWCNTs in DI water due to the carboxylic (–COOH) functional groups covalently attached to the openings as well as the sidewalls. The chemical treated SWCNTs were diluted with DI water with a concentration of 1 mg/ml.

The SWCNT-based TFTs were built on a standard 4 in. silicon wafer with a layer of 300 nm thick SiO_2 on the surface. First, chromium (Cr, 100 nm) and gold (Au, 200 nm) layers were deposited on the wafer by electron-beam evaporation. Next, a layer of photoresist was spin coated on the surface and patterned with photolithography. Wet etching was used to etch away the unwanted Cr and Au to form the source/drain electrodes. Following the wet etching and removing the remaining photoresist, a second photolithography was conducted to open a window directly above the channel region. Prior to the LBL self-assembly process, the wafer was put into the O_2 plasma for 30 s to clean the photoresist residue from the window opening. The wafer was then alternately immersed in aqueous PDDA and PSS solutions, in a sequence of [PDDA (10 min)+PSS (10 min)]$_2$. These two (PDDA/PSS) bilayers served as the precursor layers that helped to enhance the subsequent adsorption of SWCNTs and nanoparticles. Following the precursor layers, SWCNTs and SiO_2 nanoparticles were coated on the entire surface of the wafer in a sequence of [PDDA (10 min)+SWCNT (15 min)]$_5$+[PDDA (10 min)+SiO_2 (4 min)]$_6$ to produce an organized "sandwich" structure of semiconducting SWCNT multilayer and insulating SiO_2 nanoparticle multilayer. Figure 2(a) shows the schematic diagram of the LBL self-assembled SWCNT/SiO_2 layers. The self-assembled SWCNTs are shown in Fig. 2(b). Next, a layer of aluminum (Al, 110 nm) was electron-beam evaporated on the wafer to serve as the gate electrode. Finally, the wafer was soaked into the acetone solution for lift-off. Figure 2(c) shows the cross-sectional scanning electron microscope (SEM) image of the assembled thin film, which consists of a SWCNT multilayer, a SiO_2 multilayer, and an Al layer. The SWCNTs and SiO_2 nanoparticles are closely packed in the thin film. The channel width and length of the fabricated transistor were 500 and 50 μm, respectively.

Compared with a standard metal-oxide-semiconductor field-effect transistor (MOSFET), the SWCNT TFT has the same MOS (Al–SiO_2–SWCNT) structure and three terminals designated as source, drain, and gate. In addition, similar to the MOSFET, the SWCNT TFT has the current flowing through the channel controlled by a gate voltage V_G. When no voltage is applied to the gate, the current between source and drain is very small. When a negative voltage V_G is applied to the gate, positive carriers (holes) are induced in the semiconducting layer below the SWCNT-SiO_2 interface. Increasing the gate voltage V_G enhances the accumulation of holes and the conductivity of the channel. Therefore, the theory for traditional silicon MOSFET is still effective and can be used to analyze the electrical characteristics of the SWCNT TFT. As a result, the drain current I_D between source and drain can be expressed as[16]

$$I_D(\text{linear}) = \frac{WC_i\mu}{L}\left[(V_G - V_{\text{th}})V_D - \frac{1}{2}V_D^2\right], \quad (1)$$

$$I_D(\text{saturation}) = \frac{WC_i\mu}{2L}(V_G - V_{\text{th}})^2, \quad (2)$$

where I_D(linear) and I_D(saturation) are the drain currents at the linear region and the saturation region, respectively; W is the channel width; L is the channel length; C_i is the capacitance per unit area of the gate insulating layer; μ is the carrier mobility in the semiconducting layer; and V_G, V_D, and V_{th} are the gate voltage, drain-source voltage, and threshold voltage, respectively.

Both drain current I_D and accumulated charge per unit area $Q=V_GC_i$ are proportional to V_G and $C_i=\varepsilon_0\varepsilon_r/d$, where ε_0 is the permittivity of free space, ε_r is the relative dielectric constant, and d is the thickness of the insulating layer. To increase I_D and Q, materials with higher dielectric constant, thinner insulating film, or higher gate voltage can be used. The dielectric constant of the SiO_2 nanoparticle film produced by LBL self-assembly is 6,[17] which is 53.8% higher than that of the SiO_2 film produced by thermal oxidation (3.9). The increased dielectric constant is caused by the presence of intermediate polymer layers, as shown in Fig. 2(a), which have very high dielectric constants in the range of 30–120.[18] The increased dielectric constant enables more efficient charge accumulation in the semiconducting channel. It also reduces the requirements of film thickness and gate voltage.

In SWCNT TFT, the drain current I_D is controlled by the applied gate voltage V_G. Early study shows that the majority carriers in pristine semiconducting SWCNTs are holes, i.e., SWCNT is a p-type material.[19] Therefore, the p-type SWCNT TFT usually operates in the accumulation mode with a negative drain voltage V_D and negative gate voltage V_G. The fabricated SWCNT TFTs were characterized using a semiconductor parameter analyzer (HP 4156A) in the atmosphere at room temperature. Figure 3(a) shows the drain current-voltage (I-V) characteristics of a SWCNT TFT, which has a channel length $L=50$ μm and a channel width $W=500$ μm. The absolute value of drain current $|I_D|$ increases with higher $|V_G|$. This indicates the gate field effect and a p-type TFT device. Figure 3(b) shows the gate transfer characteristics of the same device with drain voltage fixed at $V_D=-5$ V. The left and right y axes represent $(-I_D)^{1/2}$ and I_D, respectively. The threshold voltage $V_{\text{th}}=-3$ V is obtained

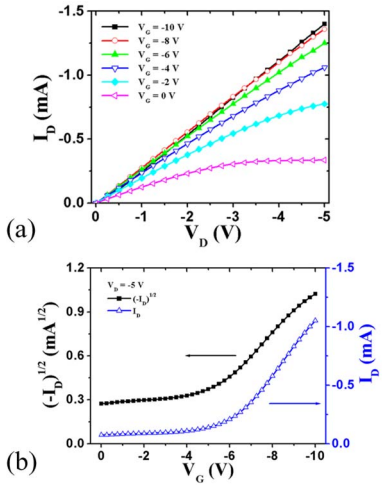

FIG. 3. (Color online) (a) Drain current-voltage characteristics of a SWNCT TFT. The gate voltage V_G sweeps from −10 to 0 V with a 2 V step. (b) Gate characteristics of the same device at the saturation region. The drain voltage V_D is fixed at −5 V. The gate voltage V_G sweeps from 0 to −10 V with a −50 mV step.

by linearly extrapolating the gate transfer curve to the V_G axis. The transconductance in the saturation region is obtained by measuring the slope of the curve, $g_m = dI_D/dV_G = 0.25$ mS. The normalized transconductance is thus derived as $g_m/W = 0.5$ S/m, which is the same as another recently reported SWCNT TFT (Ref. 7) and 50 times higher than amorphous-Si TFTs.[20]

The effective thickness of a (PDDA/SWCNT) bilayer is approximately 7.6 nm, which is obtained using a surface profiler and an ellipsometer. Therefore, the thickness of five (PDDA/SWCNT) bilayers is 38 nm. Due to the surface coverage coefficient of nanoparticles (~70%) and the air-filled pores, the effective thickness of a (PDDA/SiO_2) bilayer is 30 nm,[14] which is less than the diameter of the SiO_2 nanoparticles of 45 nm. For a dielectric film containing six (PDDA/SiO_2) bilayers, the effective thickness is $d = 180$ nm. The insulating layer capacitance/area is calculated as $C_i = \varepsilon_0\varepsilon_r/d = 2.95 \times 10^{-8}$ F/cm^2. Therefore, the hole mobility (μ_p) is calculated as 168.5 cm^2/V s from Eq. (2).

From Fig. 3(b), the on/off current ratio ($I_{on/off}$) is approximately 4.2. This value is relatively low compared with other reported high-mobility ($\mu_p > 10$ cm^2/V s) SWCNT TFTs, which typically have on/off ratios of ~100.[5–7] The low on/off ratio is caused by high off-state current, which results from the following sources. First, the high off-state current is caused by the dense network of SWCNTs in the semiconducting layer. Due to their high-aspect-ratio structures, the SWCNTs are easily wrapped together and connected to other tubes. The connection also occurs between SWCNTs from different layers. The dense SWCNT network provides high conductivity to the channel; however, it also increases the off-state current. Second, the number of assembled SWCNT layers influences the degree of interconnection. The conductivity of the thin film increases with increased number of assembled SWCNT layers. Third, the high off-state current is caused by the metallic SWCNTs in the semiconducting layer. Based on the diameter and the chirality, 2/3 of the pristine SWCNTs are predicted to be semiconducting, while the other 1/3 SWCNTs are metallic.[1] The metallic SWCNTs in the semiconducting layer can interconnect and form a highly conductive channel. Several methods may be used to overcome these problems and reduce the off-state current, for example, lowering the concentration of the SWCNT solution, shortening the immersion time, and decreasing the number of assembled SWCNT layers. The most important and effective method to reduce the off-state current is to eliminate all the metallic SWCNTs and use the primarily semiconducting SWCNTs. Several techniques have been developed to effectively separate the semiconducting tubes from the metallic tubes.[21,22]

The SWCNT TFTs fabricated with LBL nano self-assembly offer several advantages over traditional poly-Si TFTs, amorphous-Si TFTs, and organic TFTs. Poly-Si TFTs often require high processing temperature, while amorphous-Si and organic TFTs often suffer from low carrier mobilities.

In summary, we have fabricated high-mobility TFTs using LBL nano self-assembled SWCNT thin film as the semiconducting layer and SiO_2 nanoparticle thin film as the gate dielectric layer. The SWCNT TFTs operate in the accumulation mode with holes as the majority carriers. The SWCNT TFTs show high hole mobility and transconductance due to the dense network fabricated with LBL nano self-assembly. The performance of the SWCNT TFTs can be further improved by optimizing the material properties and fabrication parameters. SWCNTs, combined with LBL nano self-assembly, provide a promising method to fabricate inexpensive and high performance micro/nanoelectronic devices and integrated circuits on various substrates.

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