Applied Physics Letters

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Cite as: Appl. Phys. Lett. **87**, 183105 (2005); https://doi.org/10.1063/1.2123390
Submitted: 21 March 2005 . Accepted: 22 September 2005 . Published Online: 25 October 2005

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Field-effect transistors with layer-by-layer self-assembled nanoparticle thin films as channel and gate dielectric

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(Received 21 March 2005; accepted 22 September 2005; published online 25 October 2005)

This letter reports the fabrication of inorganic field-effect transistors (FET) combing "bottom-up" layer-by-layer (LbL) nanoself-assembly and "top-down" micromanufacturing techniques. The self-assembled multilayer of In_2O_3 and SiO_2 nanoparticles, patterned by photolithography and lift-off methods, serve as channels and insulating layers, respectively. This FET works at an accumulation mode, with a threshold voltage of −1.25 V, a carrier mobility of 4.24×10^{-3} cm^2/V s, and an on/off current ratio of 10^2. Due to the simple, low-cost, and low-temperature features of the LbL nanoself-assembly technique that greatly eliminates expensive and complex facilities, this approach is particularly suitable for the very inexpensive FET fabrication. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2123390]

Organized thin films of nanoscale particles have recently received much attention due to the recognition that they exhibit unique electronic, catalytic, and optical properties that differ from the bulk materials. They have been used as the building blocks for electronic devices,[1] microelectromechanical system devices,[2] gas sensors,[3] etc. The current methods used for the control of ultrathin films include spin coating, thermal deposition, electroplating, inkjet printing, self-assembly, etc. Self-assembly is the spontaneous organization of molecules or objects into stable, well-defined structures by noncovalent forces.[4] Among all types of self-assembly techniques, layer-by-layer (LbL) self-assembly, also called "molecular beaker epitaxy," is very promising and has caused much attraction after the pioneering work by Decher.[5] Applications of LbL self-assembly technique include electroluminescent light emitting diodes,[6] zener diode,[7] assembly of proteins,[8] conducting polymer composites,[9] etc.

Many techniques have been used to pattern polymer or nanoparticle thin film, including polymer-on-polymer stamping,[10] microcontact printing,[11] inkjet printing,[2] etc. Recently, we demonstrated the lithography approach to pattern LbL self-assembled nanoparticle thin film.[12,13] Using this approach, the metal-oxide-semiconductor capacitors based on self-assembled SiO_2 nanoparticle thin film[1] and the field-effect transistors (FETs) based on SnO_2 nanoparticle thin film[14] have been successfully fabricated and characterized. In this work, we used this approach to fabricate inorganic field-effect transistors with LbL self-assembled In_2O_3 nanoparticle thin film as the channel and SiO_2 nanoparticle thin film as the gate dielectric. In_2O_3 30 nm in diameter and SiO_2 nanoparticles 45 nm in diameter, forming the semiconductive and insulating thin films, respectively, were patterned by photolithography and lift-off processes. Immersing of the wafer into two beakers containing alternatively charged nanoparticle and polyion solutions, thin film can be grown layer-by-layer at room temperature.[12] The thickness of the adsorbed nanoparticle multilayers is in precision of 1 nm and can be monitored by the quartz crystal microbalance technique. With the combination of photolithography and LbL nanoself-assembly, highly reliable FETs with reproducible characteristics can be fabricated. The reliability, simplicity, and versatility of the newly developed processes provide an approach to many potential applications of the combination of microlithography and LbL nanoself-assembly.

Based on our previous results of self-assembled capacitors, 45 nm silica nanoparticles are selected as the dielectric material for the FET due to its reliability and uniformity. A patterned layer of titanium, 90 nm thick, serves as the source and the drain (S/D) electrodes at the bottom. Another layer of aluminum 200-nm-thick works as the gate on the top. The channel between the source and the drain is 100 μm wide and 3 μm long, which is filled with self-assembled In_2O_3 nanoparticle thin film. Figure 1 illustrates the schematic diagram of the field-effect transistor with LbL nanoassembled In_2O_3 and SiO_2 nanoparticle thin films as the active and dielectric layers, respectively. Here Al works as the gate, while Ti functions as the source and the drain.

The fabrication procedures of the FET, shown in Fig. 2, are described later. Initially, a 4 in. silicon wafer with a thin layer of SiO_2 was cleaned in a solution of sulfuric acid and hydrogen peroxide (volume ratio 3:7) at 70 °C for 1 h. Titanium S/D electrodes were deposited by sputtering, and patterned by a lithographic process [Fig. 2(a)]. Next, a layer of photoresist was spin coated on the wafer, and the windows

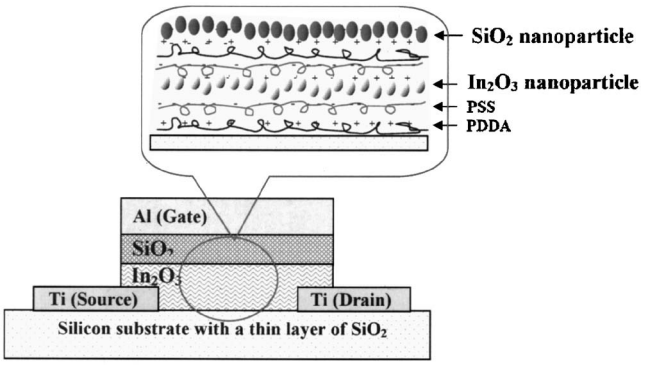

FIG. 1. Schematic diagram of the field-effect transistor with LbL In_2O_3 and SiO_2 nanoparticle thin film as functional layers.

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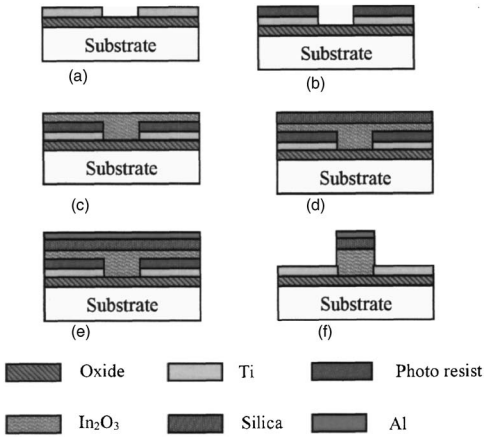

FIG. 2. Fabrication procedures of self-assembled field-effect transistors.

were open right above the channel region [Fig. 2(b)]. The wafer was then alternately immersed in aqueous poly(dimethyldiallyl ammonium chloride) (PDDA) and sodium poly(styrenesulfonate) (PSS) at a concentration of 3 mg/mL, in a sequence of $[\text{PDDA}(10\text{ min})+\text{PSS}(10\text{ min})]_3$. Here PDDA and PSS work as the precursor layers of LbL nanoself-assembly of In_2O_3 nanoparticles, while PDDA also serves as the sandwich layer between two neighboring In_2O_3 semiconductive layers. Between the immersions, there was an intermediate rinsing by de-ionized water for 1 min, followed by spin drying of the wafer at 1300 rpm for 40 s. These six layers of polyion films, about 3 nm thick, formed a uniform and strongly charged precursor layers on the wafer surface and can enhance the subsequent adsorption of nanoparticles. Following the precursor layers, In_2O_3 and SiO_2 nanoparticles in 8 mg/mL water dispersion were coated on the entire surface of the wafer in the sequence of $[In_2O_3(14\text{ min})+\text{PSS}(10\text{ min})]_4+[\text{PDDA}(10\text{ min})+SiO_2(4\text{ min})]_7$ to produce an organized "sandwich" of semiconductive nanoparticle In_2O_3 thin film and insulating nanoparticle SiO_2 thin film [Figs. 2(c) and 2(d)]. After that, a layer of aluminum 200 nm thick was evaporated on top of the surface [Fig. 2(e)]. Finally, the wafer was soaked in acetone solution with ultrasonic to perform the lift-off for 1 min [Fig. 2(f)]. Figure 3 shows the scanning electron microscopy (SEM) images of the final device and the self-assembled nanoparticle thin film. We can see from Fig. 3(b) that the LbL self-assembled nanoparticle thin film is compact and uniform.

To analyze the electrical characteristic of this inorganic FET, the theory for the silicon FET is assumed to be still effective. Thus, similar to the conventional FET, the drain current I_D in the linear region and the saturation region can be generally expressed by Eqs. (1) and (2), respectively,[15]

$$I_D = \frac{WC_j\mu}{L}\left(V_G - V_T - \frac{V_D}{2}\right)V_D, \tag{1}$$

$$I_D = \frac{WC_j\mu}{2L}(V_G - V_T)^2. \tag{2}$$

In the earlier equations, L is the channel length, W is the channel width, C_j is the capacitance per unit area of the insulating layer, V_T is the threshold voltage, V_G is the gate voltage, and μ is the field effect mobility. The accumulated charge per unit area is simply $V_G C_j$. Since $C_j=\varepsilon_0\varepsilon_r/d$, we can see that high dielectric constant materials can allow the charge to accumulate at a lower voltage. The dielectric constant of this self-assembled silica thin film was 6,[12] which is higher than the conventional silicon dioxide (3.9), because the charged polymers twisted between nanoparticles have a dielectric constant ten times higher.[16] This indicates that the self-assembled SiO_2 dielectric thin film may have advantages over the thermal oxide for the low-voltage FET.

The characteristics of the fabricated FETs were measured by Keithley system (models 236 and 238) in the atmosphere at room temperature. Figures 4(a) and 4(b) show the drain output characteristic and gate transfer characteristic, respectively. Figure 4(c) illustrates the current-voltage characteristics of the device without the overlying SiO_2 layer. The leakage current is very small and linear, which indicates that the conductivity of the channel is due to the gate field effect, where the $Ti-In_2O_3$ interface doe not dominate such a device behavior. We can see from Fig. 4(a) that the drain source conductivity increases with positive gate bias, indicating that electrons are the majority carriers in the In_2O_3 channel. Due to the existence of oxygen vacancies acting as donors, In_2O_3 is an n type semiconductor.[17] Therefore, this FET works at the accumulation mode instead of inversion mode, with nanoassembled In_2O_3 as the active layer. Increasing the gate voltage will result in the accumulation of electrons in In_2O_3 layer, and hence, increase the channel conductivity. Drain current saturation can be observed at drain voltage higher than 5 V, which means that a pinch-off of the channel occurs in the vicinity of the In_2O_3/SiO_2 vicinity. The threshold voltage V_T is −1.25 V by linearly extrapolating the gate transfer curve to the V_G axis. The growth step of the In_2O_3/PDDA layer was 28 nm, therefore the thickness of 4 semiconducting layers was 112 nm. The growth step of the

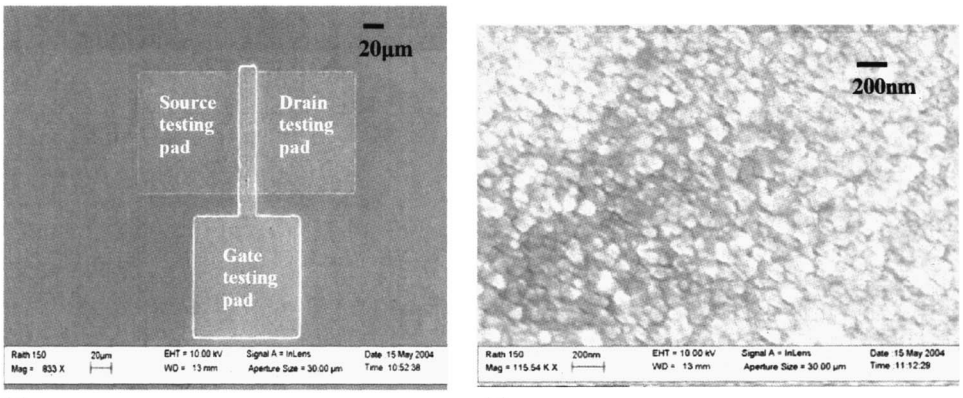

FIG. 3. The top view SEM image of (a) the final whole device and (b) the self-assembled nanoparticle thin film.

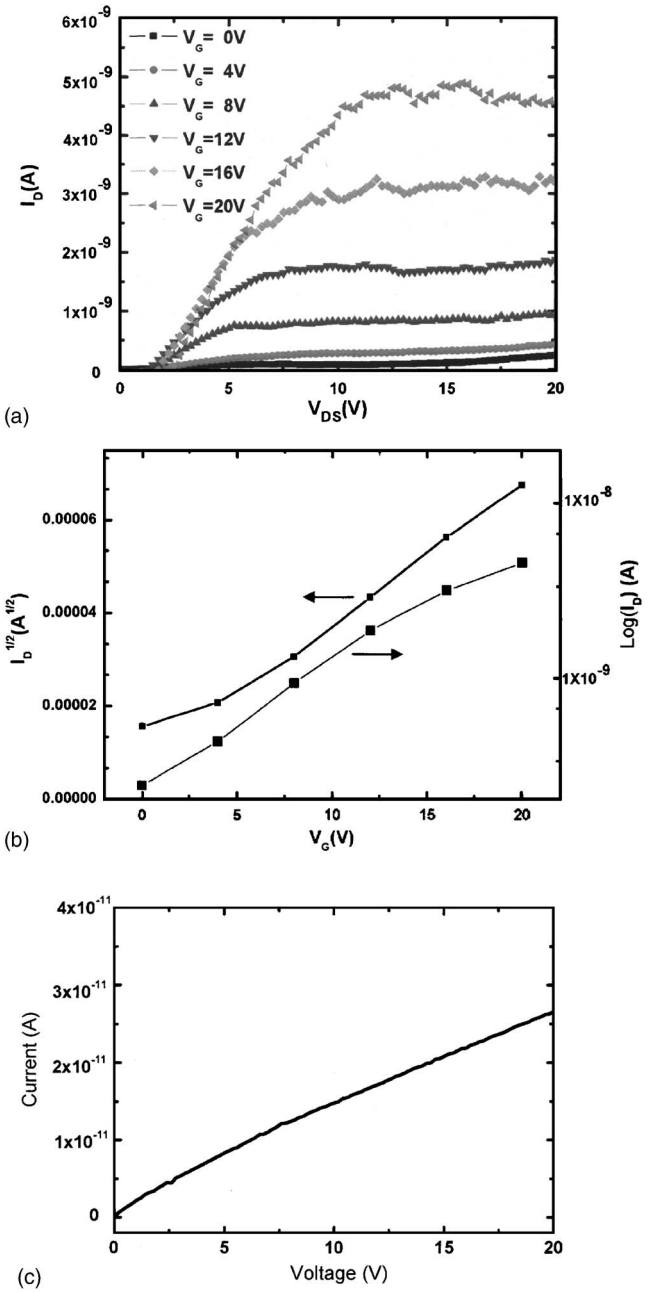

FIG. 4. (a) The drain current-voltage characteristics with gate voltages swept from 0 to 20 V. (b) The transfer characteristics with gate voltages swept from 0 to 20 V at V_D=20 V. (c) The current-voltage characteristics of the device without the overlying SiO_2 layer.

SiO_2/PDDA layer was 30 nm, hence the thickness of seven dielectric layers was 210 nm. From Eq. (2), we can calculate the saturation mobility of the FET as 4.24×10^{-3} cm^2/V s. The I_{on}/I_{off} ratio of this FET is about 10^2. The mobility of the FET is relatively low, probably because the amorphous crosslinking of the charged polyion PSS is electrostatically bonded with In_2O_3 nanoparticles, and hence hinder the electron transport in In_2O_3 thin film.

In summary, we demonstrated the very inexpensive and easy fabrication of inorganic field-effect transistors that incorporate layer-by-layer self-assembled In_2O_3 and SiO_2 nanoparticle thin films as the functional layers. Compared with the traditional silicon-based FET, our FET still has the disadvantages of low carrier mobility and on/off ratio. However, this work may provide a new approach to fabricate the low-cost micro/nanoelectronic devices and integrated circuits based on the enabling layer-by-layer nanoself-assembly technique. Further investigation and experiments to improve the performance of the nanoparticle-based FETs are on-going.

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