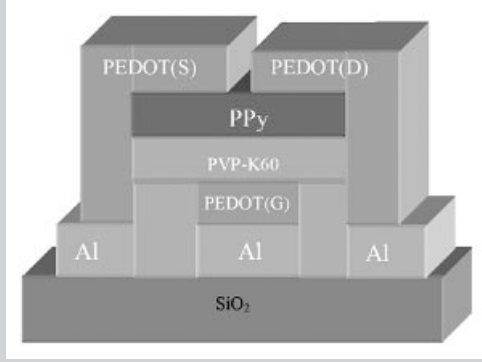
Summary: An all-polymer field-effect transistor (FET) fabricated using an inkjet printing technique is presented in this paper. Poly(3,4-ethylenedioxythiophene) works as the source/drain/gate electrode material because of its good conductivity. Polypyrrole acts as the semiconducting layer. Poly(vinyl pyrrolidone) K60, an insulating polymer with a dielectric constant of 60, operates as the dielectric layer. All the polymers are diluted with deionized water, and can be printed with a piezoelectric inkjet printing system. The device functions at a depletion mode with low operation voltage. It has a field-effect mobility of 0.1 $cm^2 \cdot V^{-1} \cdot s^{-1}$, an on/off ratio of 2.9×10^3, and a subthreshold slope of 2.81 $V \cdot decade^{-1}$.



Schematic of the all-polymer FET synthesized here.

Low-Voltage All-Polymer Field-Effect Transistor Fabricated Using an Inkjet Printing Technique

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Received: July 12, 2005; Revised: September 19, 2005; Accepted: October 20, 2005; DOI: 10.1002/marc.200500493

Keywords: all-polymer; conducting polymers; field-effect transistor; inkjet printing; low voltage

Introduction

The discovery of conducting polymers has been of great interest as a result of their application in microelectronic/optoelectronic devices.[1] Their advantages over conventional materials, such as silicon and germanium, include low cost and ease of processing. Organic or polymer-based semiconductors have been applied to fabricate field-effect transistors (FETs). Since the first reported organic FET in 1983,[2] there have been many on-going efforts to form organic or polymer-based FETs.[3–6] Organic or polymer-based transistors have already found application in smart pixels,[7] electronic luggage tags,[8] sensors,[9] and active-matrix light-emitting polymer displays,[10] etc.

A variety of approaches have been used to deposit conducting polymer or organic semiconductors based on the nature of those materials. The various techniques commonly employed include solution-processed deposition, such as spin coating and printing, electro-polymerization, and vacuum evaporation etc. Other techniques (soft lithography, self-assembly, and Langmuir-Blodgett) have also been applied to the fabrication of polymer-based FETs. Various printing techniques, including screen-printing,[11,12] micro-contact printing,[13] and inkjet printing (IJP),[14–16] are attracting more and more attention. Among these printing techniques, IJP is very promising because polymer devices fabricated by an IJP technique have the advantages of simplicity of fabrication, compatibility with various substrates, availability of non-contact, no-mask patterning, etc. IJP has been used to fabricate an all-polymer transistor,[14,15] polymer light-emitting diode (PLED),[16,17] an all-polymer capacitor,[18] resistor-capacitor (RC) filter circuits,[19] diodes,[20] and nanoparticle microelectromechanical systems,[21] etc.

For the reported all-polymer FET fabricated using an IJP technique,[14,15] only the gate (G), source (S), and drain (D) electrodes were printed, while other components, such as the dielectrics and active layers, were still deposited by spin coating and patterned by lithography. The operation voltage of those polymer-based FETs was also relatively high, which is not appropriate for the logic gate circuit applications that require low-voltage operation. An inkjet-printed insulating layer of a polymer-based FET has seldom been reported,

mainly because it is difficult to print out the insulating polymers, which are insoluble or soluble but easily clog the printer nozzles.[17] Our approach to overcome this problem is to use a water-soluble insulating polymer solution that can be easily printed out without clogging the nozzles. Since the charge in the polymer-based FET is proportional to both the dielectric constant and the gate voltage, the material with a higher dielectric constant allows the necessary charge to accumulate at much lower voltages.[22] Poly(vinyl pyrrolidone) K60 (PVP-K60), a water-soluble insulating polymer with a high dielectric constant of 60, meets the above requirements. Combining the printed poly(3,4-ethylenedioxythiophene)/poly(styrene sulfonic acid) (PEDOT/PSS) as the source/drain/gate electrodes, and printed polypyrrole (PPy) as the active layer, all-polymer transistors have been successfully synthesized using an all-IJP technique, and characterized.

Experimental Part

Device Fabrication

The inkjet printer employed in the device fabrication was a piezoelectric inkjet printer with an accuracy of ±5 μm (from Microdrop Company). The selection of suitable polymer solutions for IJP is very critical because the solutions have to satisfy the compatibility of inkjet heads and the reproducibility of drop dynamics.[23] The inkjet head compatibility means that the solvent will not block the head nozzles during printing, and the drop dynamics reproducibility relates to properties of the material, including correct viscosity and surface energy, to allow the reproducible formation of droplets with the same droplet volume and direction. To satisfy these requirements, polymers were selected that would dissolve in deionized water. After changing the ratio of polymer to water, the solution could be optimized for stable printing without clogging the nozzles. Figure 1 shows the chemical structure of the conducting polymer PEDOT/PSS, the doped semiconducting polymer PPy, and the insulating polymer PVP-K60 used in our FET fabrication.

The schematic of the printed all-polymer FET device is shown in Figure 2. First, a layer of aluminum 2 000 Å thick was deposited on the silicon dioxide wafer and patterned with UV lithography to form the contact pads. Next, PEDOT/PSS (Baytron P from Bayer Company) with a concentration of 10% was printed on the Al gate pad at a substrate temperature of 60 °C to form the gate electrode. The substrate temperature was adjusted to form a uniform layer during the printing process. Following that, the 15% PVP-K60 (From Sigma Aldrich Company) dispersion in water was dispensed onto the gate electrode at a substrate temperature of 80 °C. The third printing step was to dispense PPy (20% dissolved in water, from Aldrich Company) onto the PVP-K60 to form the active layer. Our experiments showed that a substrate temperature of 40 °C could help to form a uniform PPy layer after printing. Finally, the top source and drain electrodes made of PEDOT/PSS were printed onto the top of the PPy active layer and also extended to the Al source/drain contact pads under the same conditions used for printing the gate electrode. After each printing step, the wafer was heated for 20 min to remove the water completely. The channel length and width of the polymer-based FET are 100 and 1 200 μm, respectively. The thickness and roughness of the printed gate dielectric were 589 and 160 nm, respectively. They were measured with a roughness surface tester (from Veeco Inc.). The data of the dielectric constant ($k = 60$) was provided by the supplier (Sigma Aldrich).

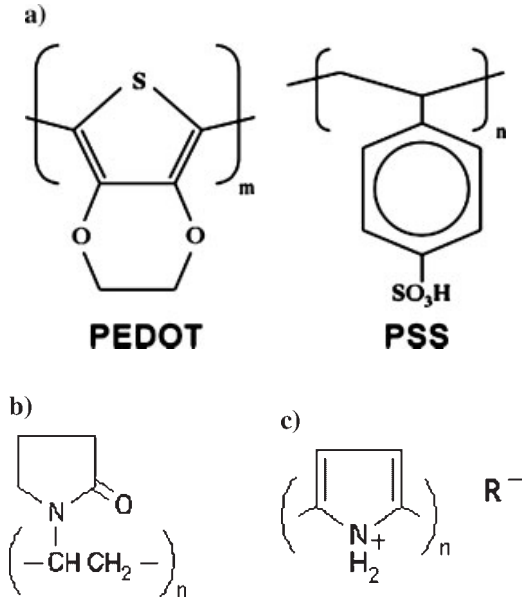

Figure 1. Chemical structures of a) PEDOT/PSS, b) PVP-K60, and c) Ppy.

Results and Discussion

For normal FETs, the drain current, I_D, increases linearly with the drain voltage, V_D, at a low V_D regime (linear regime),[24] and the relationship is expressed as:

$$I_D = \frac{WC_j\mu}{L}\left(V_G - V_T - \frac{V_D}{2}\right)V_D \quad (1)$$

where L is the channel length, W is the channel width, C_j is the capacitance per unit area of the insulating layer, V_T is the threshold voltage, V_G is the gate voltage, and μ is the field effect

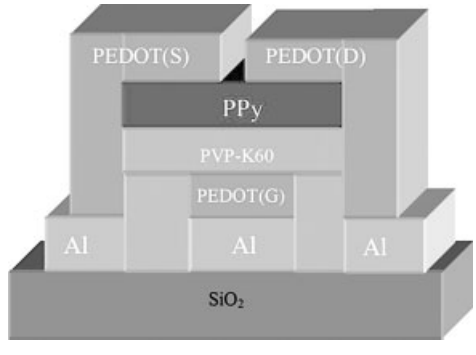

Figure 2. Schematic of the all-polymer FET.

mobility, which can be calculated in the linear regime from the transconductance given by:

$$g_m = \frac{\partial I_D}{\partial V_G}\bigg|_{V_D=\text{const.}} = \frac{WC_i}{L}\mu V_D \quad (2)$$

when $-V_D > -(V_G - V_T)$, I_D tends to saturate (saturation regime) as a result of the pinch-off of the accumulation layer, and I_D is modeled by:

$$I_D = \frac{WC_j\mu}{2L}(V_G - V_T)^2 \quad (3)$$

The accumulated charge per unit area is simply V_gC_j. Since $C_j = \varepsilon_0\varepsilon_r/d$, we can see that a polymer with a higher dielectric constant can allow the charge to accumulate at much lower voltages.

The characteristics of I_D versus V_D and I_D versus V_G of the all-polymer FETs fabricated by an all-IJP technique are shown in Figure 3a and Figure 3b, respectively. All the *I-V* measurements were implemented in the atmosphere at room temperature with the Keithley 236 source measure unit. Figure 3a shows that the device works at the linear region when the drain voltage is between -1.5 and -2.8 V, and approaches the saturation regime when V_D is larger than -2.8 V. For the region in which V_D is below -1.5 V, almost no current passes through the channel. This is mainly a result of the rectifying barrier between the Al electrode and the PEDOT S/D electrodes. Since the work function of Al (4.3 eV) is smaller than that of PEDOT (5.2 eV), a rectifying barrier (Schottky barrier) will form at the Al/PEDOT interface.[25] Therefore, an external potential is needed to overcome the Schottky barrier before the current can go through the channel. Extracted from Figure 3b, the threshold voltage is approximately -4.3 V. The on/off ratio is defined at a given negative drain bias as the ratio of the current in a transistor at its "on" state to the current at its "off" state, and can be obtained from Figure 3b at 2.9×10^3. The calculated mobility from Equation (2) is 0.1 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at $V_D = -3.5$ V. The subthreshold slope is 2.81 $V \cdot decade^{-1}$.

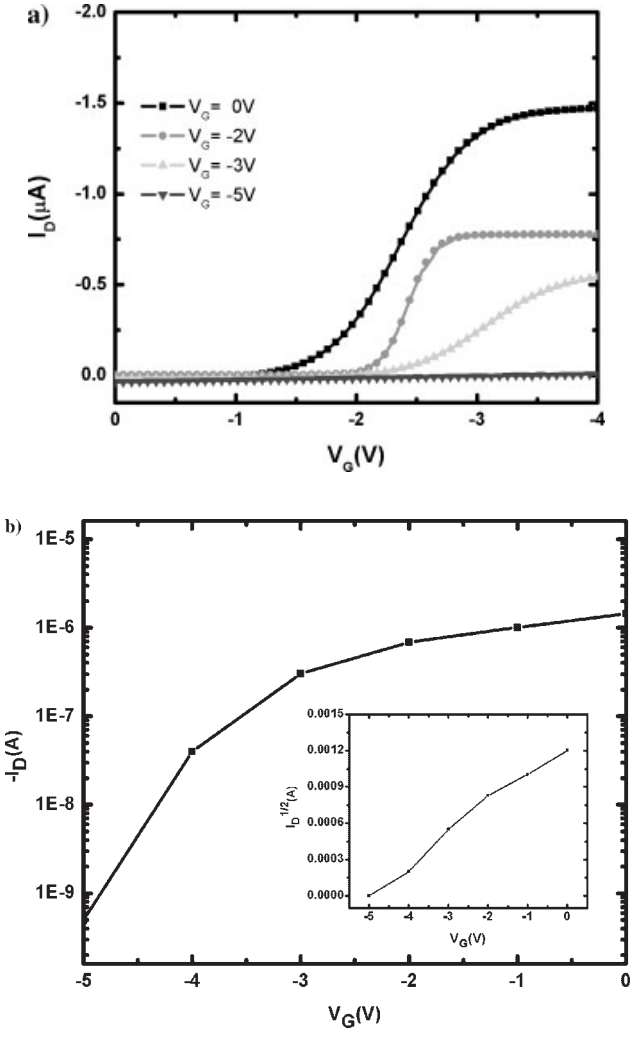

Figure 3. a) The output characteristic and b) the transfer characteristic of the all-polymer FET with PVP-K60 as the gate dielectric.

One "abnormal" behavior of this polymer-based FET is that the changing of channel conductivity affected by the gate voltage is different from most of the *p*-channel polymer-based FETs reported by other research groups. The device works as a "normally on" FET at a zero gate voltage, and falls into an "off" state when the gate voltage is increased negatively. This is contrary to the conventional definition of an "on" state where $V_G = V_D < 0$ V and an "off" state where $V_G = 0$ V when $V_D < 0$ V. To understand this "abnormal" electrical characteristic of the all-polymer FET, the device structure, the active material, and the charge transport in the polymer FET need to be considered. For the *p*-type semiconducting polymer PPy, there are two types of positive charges in the channel region, namely the doping component and the field-effect component. Since the PPy employed in this FET is doped with toluenesulfonic acid, its charge transport characteristics will be greatly affected by the dopant ions. The thickness of the printed PPy active layer is 353.20 nm as measured with the roughness surface tester. It is much thicker than conventional polymer FETs, in which the active layers were deposited by thermal evaporation or spin coating and were typical less than 100 nm. Because of the large thickness of the active layer on our FET, most of the charge carriers will transport at the surface region and form the conduction channel under negative drain voltage, as shown in Figure 4a. At zero gate voltage, charges from the doping component in the PPy will transport from the source to drain electrode under negative V_D when V_D is larger than the Schottky barrier between the PEDOT/PSS and the Al electrode. When the gate voltage is increased negatively, the field-effect charge will be generated at the PPy/PVP-K60 interface because of the band bending in the semiconductor. In the meantime, the positive doping charges that transport at the surface region will be attracted to the bulk region by the negative gate bias, as shown in Figure 4b. This will result in less charge carriers at the top surface region, and hence reduce the drain current.

To confirm the above analysis of the channel formation and to verify how the dielectric material affects the operation voltage of the polymer-based FET, an all-polymer FET with the same structure and conducting/semiconducting materials, except that the insulating material is replaced with another commonly used polymer dielectric, poly(4-vinylphenol) (PVPh), with a dielectric constant of 3.6, was fabricated.[26]

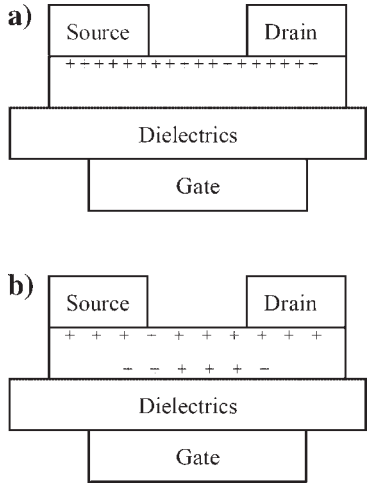

Figure 4. a) The distribution of charge carriers at zero gate voltage. b) The distribution of charge carriers when the gate voltage becomes more negative.

From Figure 5, it can be seen that this device with the same active material. i.e., PPy, and made by the IJP technique works at an operation voltage more negative than −15 V. The device also works at an ''on'' state at the zero gate voltage and falls into an ''off'' state at a less negative gate voltage. The operational voltage for the FET with a high dielectric constant was much lower than the FET with a low dielectric constant. The low voltage operation was affected by the gate dielectric constant. Therefore, the polymer with the higher dielectric constant plays a key role in the low operation voltage of an all-polymer FET. The characteristics of this low-voltage all-polymer FET are similar to the low-voltage hygroscopic insulator field-effect transistor (HIFET) reported by Sandberg and co-workers. The mechanism that gate-field modulation of the drain current is dependent on a gate-voltage-induced drift of ions doping and de-doping in the channel of the device was proposed to explain the low-voltage operation of the HIFET.[27] However, our FET has a reversed conductivity affected by gate voltages, therefore, a new mechanism based on the channel thickness and transportation position should be proposed to explain the ''abnormal'' behavior. Regarding the pinch-off of drain current at the zero gate voltage when V_D is larger than −3 V, it can still be explained by Sandberg's ion drift mechanism. When the gate voltage is close to 0 V, the drift of mobile ions in the gate dielectric layer reaches pinch-off at the drain contact and the drain current is modulated by shifting electric charge close to the semiconductor interface.

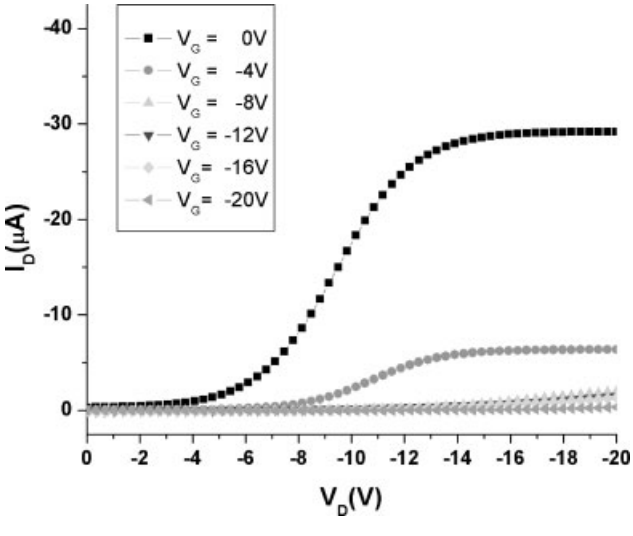

Figure 5. The output characteristic of a polymer FET with PVPh as the gate dielectric.

Conclusion

We have fabricated an all-polymer field-effect transistor using an all-inkjet printing technique. Thanks to the dielectric polymer with a high dielectric constant, the all-polymer FET operates at a low voltage. Since the printed active layer, PPy, is doped and much thicker than that using other deposition methods, this FET has a reversed gate effect conductivity. A mechanism based on the channel thickness and doping charge components has been proposed to explain the new phenomena. As far as we know, this is the first report of an all-inkjet printed all-polymer FET with a low operation voltage. Our findings can make a great contribution to the fabrication of practical polymer microelectronic devices and circuits using a simple all-inkjet printing technique.

Acknowledgements: This work is partially supported by the *DARPA* (grant no. DAAD19-02-1-0338) and the *CEnIT* seed grant at the Louisiana Tech University.

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