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Temperature and field dependent mobility in pentacene-based thin film transistors

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Abstract

Pentacene-based thin film transistors (TFTs) have been fabricated and analyzed to investigate the temperature and electric field dependence of hole mobility. At room temperature, the TFT device characteristics have displayed the hole mobility of 0.26 cm^2/V s, threshold voltage of −3.5 V, subthreshold slope of 2.5 V/decade, and on/off ratio of 10^5. Over the temperature range of 300–450 K, the hole mobility is found to increase to a peak value, followed by decrease to very low values. Similar behavior has also been observed in TFTs fabricated at a higher pentacene deposition rate. However, in this case over 20 times reduction in the extracted hole mobility values has been observed, due to the less ordered layered structure of the pentacene film present. No annealing effects have also been observed up to a temperature of about 410 K. The field dependence of hole mobility has also been evaluated at room temperature, and observed to noticeably increase with increase in electric field, over the biasing conditions considered.

Keywords: Pentacene thin film transistors; Mobility

1. Introduction

Over the past two decades organic microelectronics and optoelectronics have increasingly gained more attention due to the attractive properties and applications of organic materials [1,2]. Pentacene is one of the most investigated organic materials due to its reported high performance [3]. Pentacene-based devices such as Schottky diodes [4,5], thin film transistors (TFTs) [6–8], and integrated circuits [9,10], have been realized, and the electrical properties, as well as the magnetic properties [11] of pentacene have been studied. Technology computer-aided design (TCAD) based simulations [12,13] have also been performed to model the pentacene-based devices. Of the parameters affecting device performance, mobility is the key parameter of interest, which is a measure of the ease of charge transport in semiconducting materials. Currently the highest reported mobility in pentacene appears to be 3 cm^2/V s [14]. While the effects of temperature and electric field on mobility have been discussed in [12,15] for pentacene, and in [16–18] for other organic materials, much remains to be done to fully understand and characterize the mechanisms of charge transport in organic materials. In this work, the temperature dependence of the hole mobility in pentacene has been studied over the range of 300–450 K. The effect of pentacene deposition rate on the hole mobility has also been investigated. Moreover, the electric field dependence of hole mobility has been examined, and field dependent mobility evaluated for the TFTs with different pentacene deposition rates.

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2. Experimental

The schematic structure of the fabricated devices is shown in Fig. 1. First, heavily-doped n-type silicon wafers were prepared and cleaned as gate electrode as well as substrate. Then 100 nm-thick layer of SiO_2 is grown on silicon by thermal oxidation, and serving as gate dielectric material. Subsequently, a layer of Au/Ti (80 nm/30 nm) is deposited by sputtering, followed by photolithography and wet etching to pattern the Au/Ti source and drain (S/D) contacts. Pentacene (Aldrich, without purification) is then deposited on the channel (75 μm length and 1000 μm width) and S/D regions by thermal evaporation at 1×10^{-6} Torr through shadow mask. By holding the substrate at room temperature, pentacene thin film (200 nm) is grown at two different deposition rates of about 4 Å/s and 8 Å/s, respectively. The fabricated devices were tested with a Keithley Test System (236 source measure unit with model H1001 heat control module) at atmospheric ambient condition. The output and transfer characteristics of the fabricated pentacene TFTs have been measured, while sweeping the temperature from 300 to 450 K and then sweeping it back to observe annealing effects.

3. Results and discussion

3.1. Device performance

The output and transfer characteristics of pentacene TFT, measured at room temperature, are shown in Fig. 2. These results are for the TFT at lower deposition rate. Analogous results have also been measured for the TFT at higher deposition rate, as shown in Fig. 3. Generally the following two conventional equations for inorganic transistors are employed to describe the behavior of organic transistors [19,20]:

$$I_{ds} = \frac{wC_i}{L}\mu\left(V_{gs} - V_{th} - \frac{V_{ds}}{2}\right)V_{ds} \quad \text{(Linear-region);} \tag{1}$$

$$I_{ds} = \frac{wC_i}{2L}\mu(V_{gs} - V_{th})^2 \quad \text{(Saturation-region).} \tag{2}$$

Based on the above equations and experimental data, the device parameters for the pentacene TFTs have been

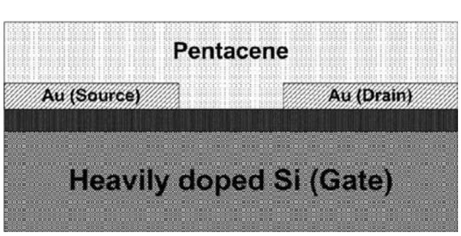

Fig. 1. Schematic structure of fabricated pentacene TFTs.

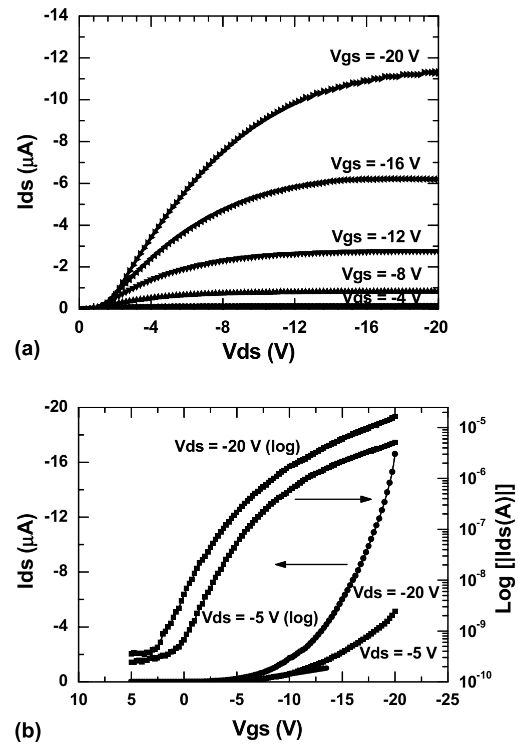

Fig. 2. Output characteristics (a) and transfer characteristics (b) of pentacene TFT with 75 μm channel length and 1000 μm channel width, measured at room temperature. Pentacene has been thermally evaporated at 1×10^{-6} Torr and at lower deposition rate (4 Å/s) with the thickness of 200 nm.

extracted, resulting in saturation hole mobility of 0.26 cm^2/V s, threshold voltage of −3.5 V, subthreshold slope of 2.5 V/decade, and on/off ratio of 10^5 for the device with lower deposition rate (Fig. 2). For the pentacene TFTs at the higher deposition rate, hole mobility is 0.003 cm^2/V s, a threshold voltage of 2.5 V, a subthreshold slope of 6 V/decade, and an on/off ratio of 10^3, as shown in Fig. 3. Since pentacene is the only active material in the TFTs, the performance is mostly determined by the charge transport in pentacene and the interfaces of pentacene/Au and pentacene/SiO_2. The ability of charge transport in pentacene is affected by processing conditions, including the deposition pressure, and substrate conditions [21,22]. In the following section, it is shown that the hole mobility also appears to be related to deposition rate.

3.2. Temperature dependence

Mobility is the key device parameter affecting performance in TFTs. The extracted plot of the hole mobility as a function of temperature is shown in Fig. 4. It is found that over the temperature range of 300–450 K, the hole mobility increases to a peak value and then decreases to very low values. Previous experiments and

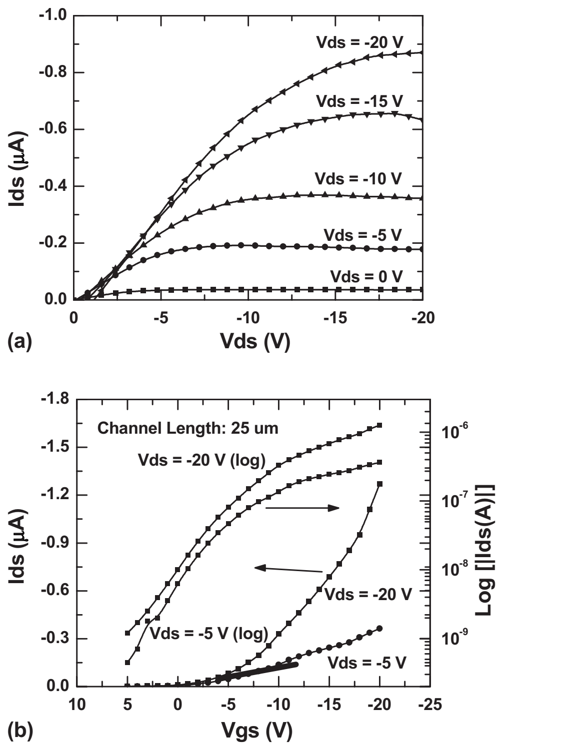

Fig. 3. Output characteristics (a) and transfer characteristics (b) of pentacene TFT with 25 µm channel length and 800 µm channel width, measured at room temperature. Pentacene has been thermally evaporated at 1×10^{-6} Torr and at higher deposition rate (8 Å/s) with a thickness of 200 nm.

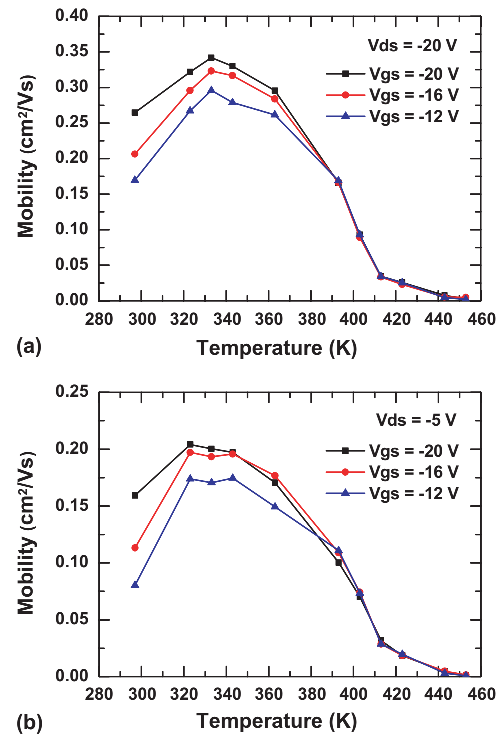

Fig. 4. Temperature dependent mobility at $V_{ds} = -20$ V and $V_{ds} = -5$ V for different gate voltages for pentacene TFTs at lower deposition rate (4 Å/s).

analyses have indicated that thermally activated hopping transport occurs in some organic materials below room temperature [16,23]. Here, the hole mobility increases with temperature, displaying an Arrhenius behavior. But above room temperature, as the temperature is increased, the mobility in pentacene eventually decreases. This is attributed to the higher carrier scattering occurring at more elevated temperatures. Scattering phenomena increasingly dominate the behavior of transistors and thus determine the performance of the devices with the increase in temperature. Moreover, at higher temperatures, eventually pentacene ceases acting as an active material. As illustrated in Fig. 5, by fabricating the TFTs with higher pentacene deposition rate, a similar type of result and behavior is obtained as in Fig. 4, except that there is over 20 times reduction in the extracted hole mobility values. This is attributed to the change in the structure and morphology of the deposited pentacene layer, where higher deposition rate has resulted in less ordered layered structure of the pentacene film. For the TFTs considered, it has also been observed that by sweeping back the temperature and re-testing the devices again, almost the same device characteristics are measured up to a temperature of about 410 K, demonstrating no apparent annealing effects below this temperature.

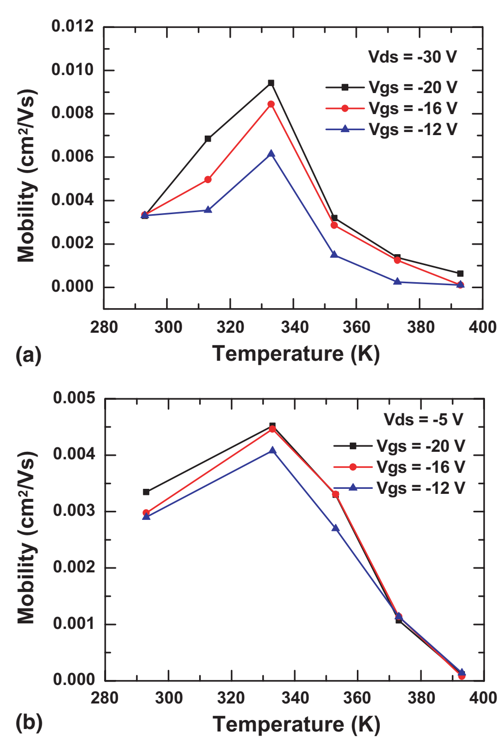

Fig. 5. Temperature dependent mobility at $V_{ds} = -30$ V and $V_{ds} = -5$ V for different gate voltages for pentacene TFTs at higher deposition rate (8 Å/s).

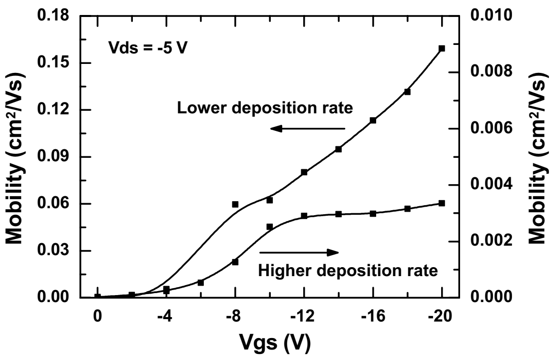

Fig. 6. Gate voltage dependent mobility in pentacene TFTs at room temperature at $V_{ds} = -5$ V. The two sets of results presented are for TFTs fabricated at deposition rates of about 4 Å/s and 8 Å/s, respectively.

3.3. Field dependence

The electric field dependence of hole mobility has also been examined in this study. When the drain voltage-generated lateral electric field is weak, the vertical electric field due to gate voltage can strongly influence the hole mobility. According to Eq. (1) and its differential [24],

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{wC_i}{L} \mu V_{ds}, \tag{3}$$

where g_m is transconductance. Using the above equation and experimental data, the field dependence of mobility can be determined. Fig. 6 shows the field dependent hole mobility in pentacene TFTs at room temperature and $V_{ds} = -5$ V. The two sets of results presented are for TFTs fabricated at lower and higher deposition rates, respectively. In both cases the mobility is noticeably increased by the increase in electric field at higher gate voltages, while, as observed earlier, the pentacene deposition rate also plays a major role in influencing mobility.

Unlike inorganic semiconductors, pentacene show increase in mobility with increase in the gate voltage, as shown in Fig. 6. This phenomenon is also reported in [17,25] for polycrystalline sexithiophene (6T). This gate voltage dependent mobility is attributed to the trapping of charge carriers by the interfacial and bulk traps at lower values of the gate voltage [26,27]. As the gate voltage increases and more traps are filled, additional charge carriers move more freely through the channel, resulting in increase in mobility.

4. Conclusions

Temperature and electric field dependence of hole mobility in pentacene thin film transistors has been studied. At room temperature, the TFT device characteristics have displayed the hole mobility of 0.26 cm^2/V s, threshold voltage of -3.5 V, subthreshold slope of 2.5 V/decade, and on/off ratio of 10^5. Over the temperature range of 300–450 K, mobility is found to increase to a peak value, followed by decrease to very low values. The increase in the hole mobility at lower temperatures is consistent with the presence of thermally activated hopping transport mechanism, and the decrease in the hole mobility at higher temperatures is attributed to the increased level of carrier scattering. Similar behavior has also been observed in TFTs fabricated at a higher pentacene deposition rate, except that over 20 times reduction in the extracted mobility values has been observed. No annealing effects have also been observed up to a temperature of about 410 K. The electric field dependence of hole mobility has also been examined at room temperature, and observed to noticeably increase with increase in electric field, over the biasing conditions considered.

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