FET Fabricated by Layer-by-Layer Nanoassembly

Tianhong Cui, Feng Hua, and Yuri Lvov

***Abstract*—Metal-oxide-semiconductor field-effect transistor (MOSFET) arrays are fabricated on a 4-in silicon wafer by the combination of conventional microelectronic processes and layer-by-layer nanofabrication. The active and insulating layers were self-assembled as organized multilayers of 15-nm diameter SnO_2 and 45-nm diameter SiO_2 nanoparticles, respectively. The source, drain, and gate electrodes are made of metal thin films. The threshold voltage is 3 V, on-off current ratio 10^4, and mobility 2.1 $\times 10^{-2}$ cm^2/V $\cdot$ s. This prototype leads to a new approach to fabricate low-cost MOSFETs and integrated circuits based on the layer-by-layer self-assembly of nanoparticles and charged macromolecules.**

***Index Terms*—Field-effect transistor (FET), lithography, nano self-assembly, nanoparticle.**

I. Introduction

Nanoparticles are attracting more and more attention due to their interesting electronic, catalytic, and optical properties, which can be finely tuned by varying their size [1]–[9]. Different types of functional nanoparticles are promising materials as the building blocks for microelectronics, optoelectronics, and catalysis. Of special interest are the technologies bridging the gap between the bottom-up nanoassembly and the top-down micromanufacturing. In such processes, massive parallelism must be implemented to achieve industrial-scale productivity [10]. In this brief, we integrated traditional planar microfabrication techniques, such as lithography and sputtering, with the assembly of nanoparticles in the third (vertical) direction.

Layer-by-layer (LBL) self-assembly is a prospective nanofabrication technique to design precisely organized multilayer structures by putting together different nanoblocks, both organic and inorganic [11]. The layered structures are realized by the alternate adsorption of oppositely charged macromolecules or nanoparticles via an electrostatic attraction. The assembly growth step perpendicular to a substrate may be controlled with the precision of 1 nm, and a number of the monolayers in the film can be precisely 1, 2, 3, 4, or more. Any type of charged nanoparticles can be coated on a solid substrate by alternate adsorption with oppositely charged linear polyions [11]–[17]. Applications of LBL nanoparticle/polycation multilayers to CdTe electro-optical devices, Schottky-diodes at the TiO_2/Au interface, and montmorillonite modified lithium batteries are demonstrated. [15]–[17].

Patterning of LBL-assembled nanoparticles in the planar direction for their integration into viable systems is critical for micro/nanodevices, such as nanoelectronic chips or nanoelectromechanical systems (NEMS) [5], [18]–[22]. Vargo *et al.* patterned polymer multilayers by controlled adhesion of linear polyions to plasma-modified fluoropolymer surfaces [23]. Yang and Rubner presented the microprinted lines 300 μm wide on hydrogen-bond-based LBL multilayers with ink-jet printer [24]. Hammond *et al.* demonstrated the patterning of one- or two-type nanoparticles assembled with LBL technique using microstamping technique [25] and [26]. In our earlier reports, an approach based on the combination of lithography and LBL nanoassembly was presented to pattern one or two types of nanoparticles on 4-in silicon wafers [27]–[29].

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II. Experiments

In this brief, 15-nm diameter SnO_2 and 45-nm diameter SiO_2 nanoparticles, constituting the semiconductive and insulating thin films, were patterned by the conventional lithography and lift-off processes. The thickness of the adsorbed nanoparticle multilayers was adjusted with precision of a few nanometers. The equipment required for nanoassembly was a dipping robot (Rigler and Kirstein, Germany), and the process was carried out by alternate immersions of the wafer into two beakers containing nanoparticle and polycation solutions at room temperature. The simplicity and versatility of the newly developed process provide a way to the potential commercialization of the approach combining microlithography with LBL nanoassembly.

We reported earlier the fabrication and characterization of a MOS capacitor [29], whose insulating layer was realized by the assembly of six layers of 45-nm silica (totally about 240 nm thick). The precision of the geometrical sizes of the device was 1 nm in the vertical direction and 1 μm in the plane. Its electronic characteristics were reliable, showing distinct accumulation, depletion, and inversion regions in the capacitance–voltage (*C-V*) curve. This proves that the LBL self-assembled silica nanoparticle thin film can operate in devices in the same way as the silicon dioxide by conventional thermal oxidation. The dielectric constant of this silica thin film was 6, which is higher than 3.9 for the conventional silicon dioxide because the charged polymers twisted between any two layers of nanoparticles has a dielectric constant ten times higher [30].

Based on the above results, we selected the 45-nm silica particles as the dielectric material for the MOSFET. A patterned layer of 90-nm-thick titanium serves as the source and drain electrodes and another patterned layer of 200-nm-thick aluminum as the gate. The channel between the source and the drain is 100 μm wide and 5 μm long and is filled with 15-nm-diameter SnO_2 particles (Fig. 1).

The procedures of the MOSFET fabrication are described as follows. Initially, a 4-in silicon wafer with a thin layer of thermal oxide is soaked in sulfuric acid and hydrogen peroxide solution (volume ratio 3 : 7) at 70 °C for 1 h. The source and drain electrodes made of titanium (90 nm thick) were deposited by sputtering and patterned by a lithographic process. Next, photoresist is spun on the wafer to pattern the windows right above the channel region. The wafer is alternately immersed in aqueous poly(dimethyldiallyl ammonium chloride) (PDDA, MW 200 000, Sigma) and sodium poly(styrenesulfonate) (PSS, MW 70 000, Sigma) at a concentration of 3 mg/mL and pH 8, in a sequence of $[\mathrm{PDDA}(10\ \mathrm{min}) + \mathrm{PSS}(10\ \mathrm{min})]_2$. The subscript 2 here designates the number of immersion, i.e., PDDA and PSS films were coated twice on surface. Between the two immersions, there was an intermediate rinsing by deionized water for 1 min followed by spin drying the wafer at 1300 r/min for 40 s. These four layers of polyion films enhanced the subsequent nanoparticle adsorption because they form a uniform and strongly charged 3-nm-thick precursor on the wafer surface. Following the precursor layers, 15-nm SnO_2 and 45-nm SiO_2 nanoparticles, taken at 8 mg/mL and pH 8 water dispersion [30], were coated on the entire surface of the wafer in the sequence

$$[\mathrm{PDDA}(10\ \mathrm{min}) + \mathrm{SnO_2}(10\ \mathrm{min})]_6 + [\mathrm{PDDA}(10\ \mathrm{min}) + \mathrm{SiO_2}(4\ \mathrm{min})]_6$$

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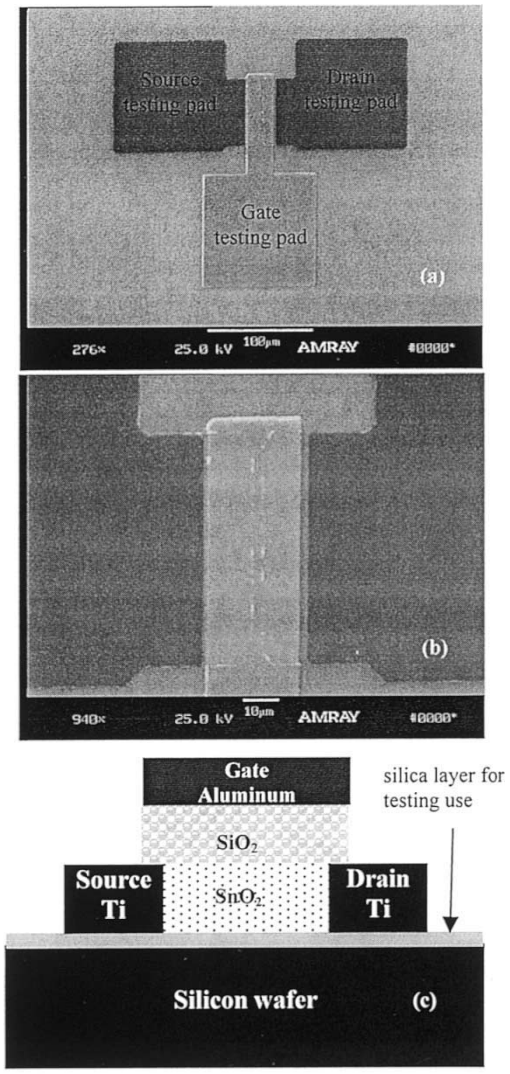

Fig. 1. (a) SEM image of a MOSFET (top view). (b) Amplified channel region. (c) Structural schematic of the MOSFET.

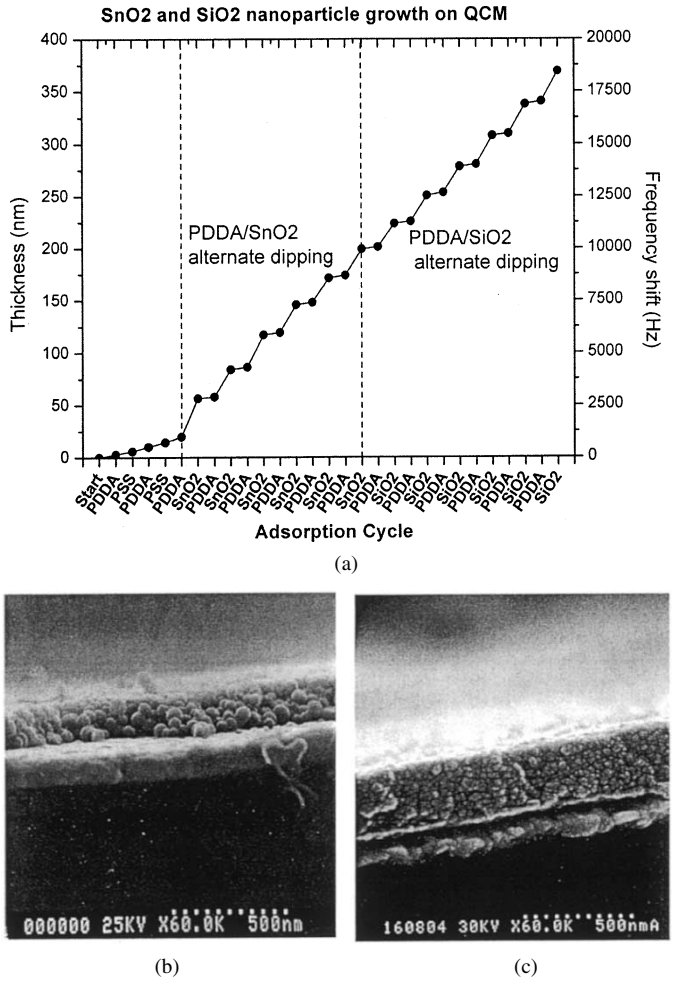

Fig. 2. (a) Adsorption of SnO_2 (15 nm) and SiO_2 (45 nm) nanoparticles on QCM, the first five steps are the precursor layer. Then, six layers of SnO_2 and SiO_2 are adsorbed in alternate with PDDA. The right vertical axis is the frequency shift, and the left one is calculated thickness. (b) and (c) SEM cross-section images of the growth of silica film. Hitachi S-5200 SEM operated at 5 kV. The sample coated with 2 nm Pt, and the substrate is silver electrode.

to produce an organized "sandwich" of semiconducting and insulating nanoparticles.[1] A layer of aluminum 200 nm thick was evaporated on the surface. Finally, the wafer was soaked in acetone solution to perform the lift-off with sonication for 5 s to cut off the links between polyions and to remove the materials above the photoresist everywhere except the gate region.

The LBL assembly process for semiconducting and insulating thin films was monitored by the quartz crystal microbalance (QCM, USI-System, Japan) technique. The QCM detects the resonance frequency shift, and it can be converted to an increment of adsorbed mass and thickness with Sauerbrey equations [32]. For the 9-MHz resonator with an effective area of 0.16 ± 0.01 cm^2, the following equation relating the frequency shift (ΔF) to the increase of thickness (d) was given by [12]:

$$d(\text{nm}) = -0.022 \times \Delta F(\text{Hz}). \quad (1)$$

The QCM resonator was immersed in a solution for a given period of time and dried in a nitrogen stream. A decrease of frequency is expected if additional mass is adsorbed onto it. The step growth monitored by QCM is shown in Fig. 2(a). The right vertical axis is the frequency shift, and the left one stands for the thickness calculated from the frequency shift. At the first stage, a well-defined precursor film containing five polyion layers in the alternate mode of PDDA/PSS was coated onto resonators. Next, the SnO_2 was adsorbed, alternating with PDDA followed by six layers of SiO_2/PDDA. This process was periodically interrupted for the purpose of measuring the QCM resonance frequency. Fig. 2(a) shows the frequency shifts and corresponding multilayer thicknesses in dependence on the adsorption steps. One can see that the growth step for the nanoparticles was much larger than the one for polyion layers.

The LBL-assembled insulating layers are shown in Fig. 2(b) and (c). The images are cross-section views of the QCM silver electrodes with those nanoparticle multilayers. One can see multilayers with closely packed nanoparticles and a smooth surface. These results demonstrate an ability to build up vertical nanoscale structures for microelectronic devices with LBL technique. The growth of the nanoparticles was linear and stable with an increment of about 30 nm for one bilayer. The polymeric PDDA interlayer thickness was of 1–2 nm. The growth step of the SnO_2/PDDA bilayer was 28 ± 2 nm, and the thickness of six bilayers was 170 nm including 25-nm precursor polymer layers. The growth step of the SiO_2/PDDA bilayer was 30 ± 2 nm, and for six bilayers this gave 180 nm. It shows that one coating of the SiO_2 nanoparticles does not completely cover the surface. The complete

[1]Aqueous dispersions of SiO_2 nanoparticles were purchased from Nissan Chemical Corporation, and SnO_2 were from Nyacol Inc.

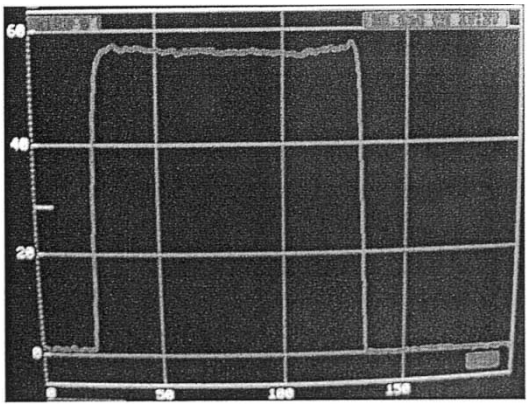

Fig. 3. Thickness measured by Tencor profilometer, about 575 nm, is in agreement with the one calculated by Sauerbrey equation. The units of the x-axis and y-axis are micrometers and $\times 10$ nanometers, respectively.

coverage should be done by more than one coating. As a result, the average step growth is smaller than the nanoparticle diameter. The total thickness of the nanoparticle sandwich layer was 375 nm as one can conclude from QCM data [Fig. 2(a)]. Including the 200-nm top aluminum layer, the total thickness of the device is 575 nm. This is in good agreement with the device thickness measured by the two-dimensional profilometer, as shown in Fig. 3.

III. Results and Discussion

The I_d–V_D drain characteristics under different gate voltages and gate transfer characteristics of the MOSFET are shown in Fig. 4. Source is the reference to which all voltages are measured. Fig. 4(a) indicates that drain currents increase linearly with drain voltages when gate voltages are small. When gate voltages increase to be more positive, drain currents rise more steeply at small drain voltages and show saturation tendency at high drain voltages. This MOSFET show two working regions: the linear region and the saturation region. Fig. 4(b) illustrates the gate transfer characteristics with gate voltages swept from 0–10 V at the drain voltage of 4 V. It shows that the drain currents increase sharply when the gate voltages are relatively small. The MOSFET has a channel length and width of 5 and 100 μm, respectively, and a dielectric thickness of 180 nm. The source and the drain are made of titanium, and the gate is formed by aluminum. The drain current increases with the gate voltages from 0–6 V at a step of 545 mV. To analyze the electrical performance of the MOSFET, we assume that the traditional theory is effective [31]. Under this circumstance, the conductive channel induced by the gate voltage is an n-channel with electrons as the carrier. By linearly extrapolating the square rooted gate transfer curve to the V_G axis, the threshold voltage $V_{\rm th}$ can be extracted to be 3 V. In the conventional theory, the drain current in the linear and saturation region can be expressed as

$$I_{\rm d}(\text{linear}) = \frac{W\mu_{\rm FET}C_i}{L}V_D(V_g - V_{\rm th}) \tag{2}$$

$$I_{\rm d}(\text{saturation}) = \frac{W\mu_{\rm FET}C_i}{2L}(V_g - V_{\rm th})^2 \tag{3}$$

where $I_d(\text{linear})$ and $I_d(\text{saturation})$ are the drain current in the linear and saturation regions, W and L are the channel width and length, $\mu_{\rm FET}$ is the carrier mobility, $V_{\rm th}$ is the threshold voltage, C_i is the gate dielectric capacitance per unit area, $2\times10^{-4} F/\text{m}^2$ in our early report (*25*). The electron mobility can be extracted to be $2.1\times10^{-2}\ \text{cm}^2/V\cdot s$ by inputting all the parameters including $I_d(\text{saturation})$ and V_D into (3). From Fig. 4(b), the on/off current ratio is about 10^4. The subthreshold slope is 1.75 V/decade. SnO_2 is an n-type, wide-band-gap

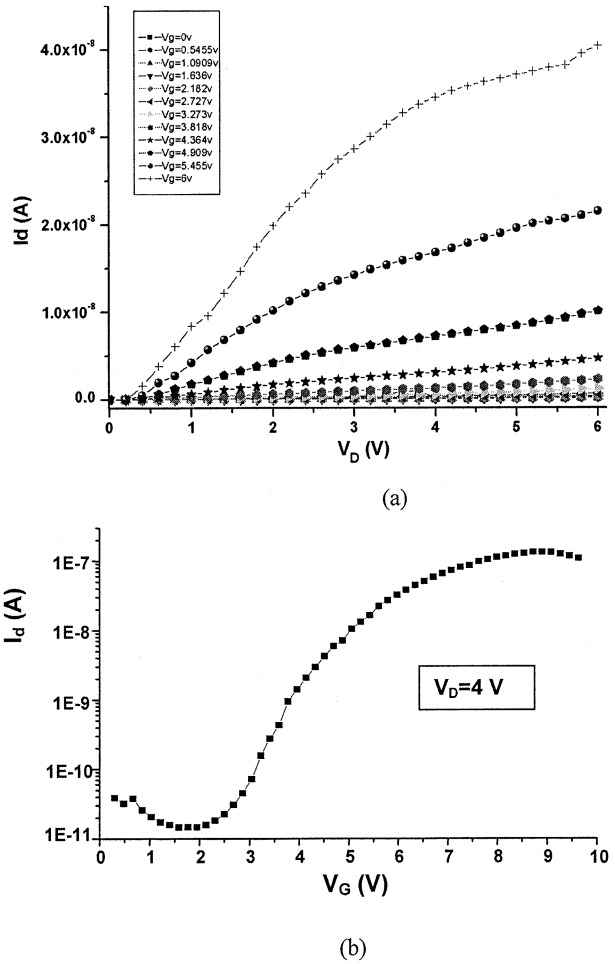

Fig. 4. (a) Drain *I–V* characteristics with gate voltages swept from 0–6 V in 0.545 V step. The channel width and length are 100 and 5 μm. (b) Transfer characteristics with gate voltages swept from 0–10 V at $V_D = 4$ V.

(Eg $= 3.6$ eV) semiconductor. The electrical conductivity of SnO_2 results primarily from the existence of oxygen vacancies, which act as donors. From Fig. 4(a), one concludes that this MOSFET is working under carrier accumulation instead of carrier inversion mode. The characteristics of this nanoparticle-based MOSFET working under carrier accumulation are similar to a polymeric MOSFET. This is probably due to the positively charged polyion (PDDA) electrostatically bonded with SnO_2, showing the electrical characteristics similar to the ones of semiconductive polymers.

IV. Conclusion

This research opens a way for the production of the low-cost micro/nanoelectronic devices and integrated circuits based on the layer-by-layer nanoassembly technique. As a prototype, this MOSFET has some problems, for example, a low on/off ratio. The operation electrical mechanism is not well understood yet. There is an avenue to optimize these devices: other nanoparticles such as TiO_2 and In_2O_3 are under investigation in our group as the active layers of the MOS transistors. The optimization of device geometry may also enhance the MOSFET properties.

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Diffusion Capacitance and Laser Diodes

John Strologas and Karl Hess

***Abstract*—The well-known diffusion capacitance is critical in determining the modulation response of p–n junctions and particularly of laser diodes. In this brief, we investigate the diffusion capacitance of a diode, as a function of the physical length of the diode and the carrier lifetimes in the narrow active region. We show that diode length and lifetime together, and not just the lifetime (which is well known), determine the bandwidth of the diode.**

***Index Terms*—Carrier lifetime, depletion capacitance, diffusion capacitance, diode length, laser diode, modulation response.**

I. INTRODUCTION

In this brief, we consider a symmetric one-dimensional (1-D) diode extending from $x = -L$ to $x = L$, where the negative x region is the

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