Fabrication and Characterization of Polymeric P-Channel Junction FETs

Tianhong Cui, Yuxin Liu, and Kody Varahramyan

***Abstract*—Polymer materials are attracting more and more attention for the applications to microelectronic/optoelectronic devices due to their flexibility, lightweight, low cost, etc. In this paper, fabrication and characterization of a polymer junction field-effect transistor (JFET), using poly (3,4-ethylenedioxythiophene) poly (styrenesulfonate) (PEDT/PSS) as the channel and poly (2,5-hexyloxy p-phenylene cyanovinylene) (CNPPV) as the gate layer, are reported. The all-polymer JFET was fabricated by the conventional ultraviolet (UV) lithography techniques. The fabricated device was measured and characterized electrically. In the meantime, the comparisons were listed between polymer JFET and analogous inorganic semiconductor counterparts. Its pinch-off voltage reaches 1 V that is in the applicable range, and the current is -13.8 μA at zero gate bias. It demonstrates that the device operates in a very similar fashion to its conventional counterparts.**

***Index Terms*—Junction field-effect transistor (JFET), microfabrication, polymer microelectronics, transistor.**

I. Introduction

POLYMERS, as one type of synthetic material, have been broadly used as anticorrosion packaging materials. As the smart materials, polymers can also be widely applied to sensors, actuators [1]–[4], artificial muscles, and electrically conducting textiles, etc. [5]. However, the most important development in the polymer world was the discovery of conducting polymers. It stimulated the polymer research and development on microelectronic/optoelectronic applications.

Since the first polymer-based transistor with polyacetylene as the active semiconductor was fabricated by Ebisawa *et al.*in 1983 [6], extensive research work has been done in the field of organic devices. In 1989, the first polymer light emitting diode (PLED) with polyphenylene-vinylene as the emissive layer was made by the University of Cambridge. In 1997, the first printed transistor in the world was developed at Lucent Technologies, Bell Labs Innovations. Furthermore, the first all-polymer transistor by ink-jet printing technique was fabricated by T. Kawase, *et al.* [7].

Ink-jet printing, optical lithography, thermal evaporation, reactive ion etching (RIE), hot embossing, self-assembly, and *in-situ* polymerization are the main techniques to fabricate polymer devices. The possibility of processing conducting polymers based on coating techniques has enabled researchers to fabricate various electronic/optoelectronic devices such as thin film transistors, diodes, LEDs, capacitors, organic integrated circuits, organic wires, and electroluminescent devices [8]–[14]. Polymer thin films can be coated on substrates such as glass, plastic, silicon, wood, or paper.

In this paper, a p-channel polymer JFET fabricated with ultraviolet (UV) lithography was presented, and its operation mechanism was discussed in detail. Based on the testing results, the polymer JFET and the characteristics of conducting polymers were analyzed.

II. Experiments

The JFET is a device providing a controlled transport of majority carriers through a semiconductor, and its key part is a nonlinear resistor fabricated with a doped semiconductor material. To be specific, we refer to it as a p-channel polymeric JFET because the conducting material is a p-type semiconductor polymer material, poly (3,4-ethylenedioxythiophene) poly (styrenesulfonate) (PEDT/PSS) (Baytron P from Bayer AG) in this paper. The gate material is an n-type polymer, poly (2,5-hexyloxy p-phenylene cyanovinylene) (CNPPV). The device was fabricated through the processes outlined in Fig. 1(a)–(d).

First, a silicon dioxide wafer covered with a layer of evaporated 0.15-μm aluminum (Al) was used as the substrate, which can also be glass or polymer materials. Two layers of polymers, 1-μm PEDOT/PSS and 1-μm CNPPV, were spun on the substrate at the bottom and on the top, respectively. Each layer was baked at 100–105°C for 1–5 minutes before the next layer was spun. Next, 0.15 μm Al was deposited on top of the CNPPV by thermal evaporation. Al, instead of photoresist (PR), was used as an etching mask layer because PR is difficult to remove selectively. After patterning of Al and Reactive Ion Etching (RIE) of CNPPV, a layer of PEDT/PSS was spun on top of the pattern to fill the channel region between the CNPPV gates, followed by another 0.15-μm-thick Al film evaporated on top of the PEDT/PSS. Finally, the clean JFET structures, as shown in Fig. 2, were built after wet etching of Al and RIE of the polymer.

Though only basic lithographic techniques applied, several issues need to be considered and avoided. One needs to control the time to etch CNPPV, and keep the PEDT/PSS from being etched. It normally takes 1 min to remove CNPPV at the condition of Table I.

Moisture inside the polymer layers can cause the polymer degradation. One approach to solve this problem is to bake and

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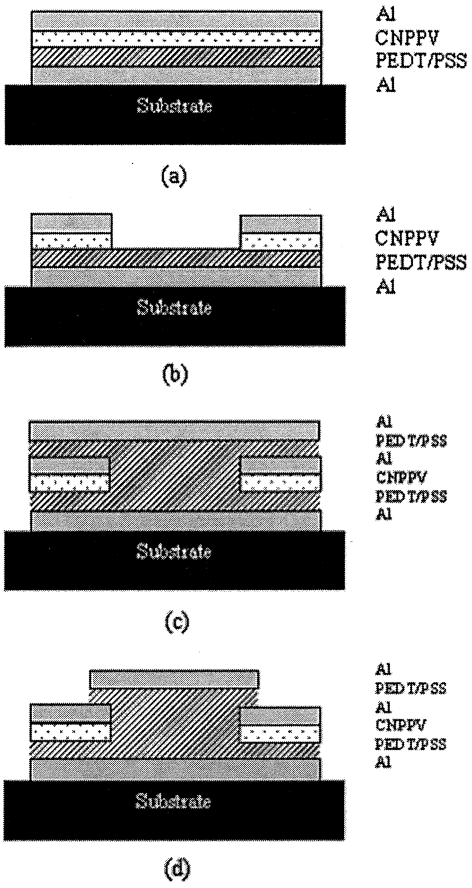

Fig. 1. Fabrication procedures of JFET.

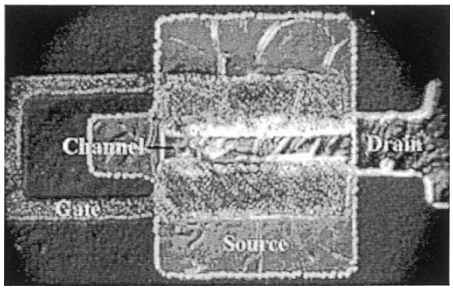

Fig. 2. JFET on the silicon substrate.

dry each layer completely prior to the fabrication of the following layers. The other way is to make the fabrication process step by step continuously to prevent moisture from the environment. Moreover, the device also needs to be baked after a long period of time between two fabrication steps. Compared with p-type polymers, the degradation of n-type polymers is much easier. In addition to working as electrical contacts, Al can be used on top of CNPPV as the passivation layer. The protecting layer of Al makes the electrical performance of the JFET more stable during a long period of time.

III. Results and Analysis

A. Drain and Transconductance Characterization

The p-channel polymeric JFET was characterized in air ambient with a Keithley Test and Measurement Instrument.

TABLE I
CONDITIONS FOR REACTIVE ION ETCHING OF CNPPV

Oxygen	Power	Pressure
20sccm	200w	<10mTorr

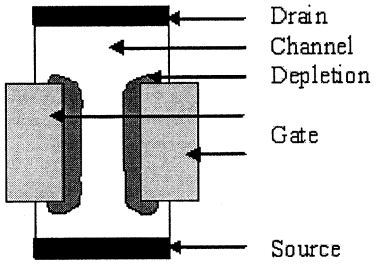

Fig. 3. JFET structure.

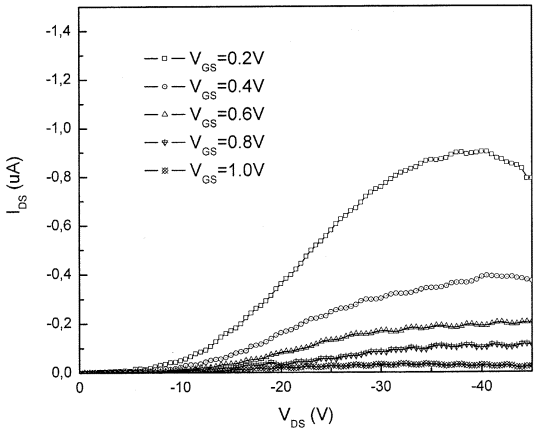

Fig. 4. Drain characteristics of a p-channel polymeric JFET.

Keithley software provides comprehensive analysis to the measured and calculated parameters. Fig. 3 shows the schematic structure of the JFET, which can be explained by the mechanism of conventional JFETs.

The JFET makes use of the fact that a very strong electric field exists across a pn–junction, and the electric field effectively removes carriers from the junction region. The gate electrodes shown in Fig. 3 are formed as pn–junctions, with the channel forming between two junctions. Two identical positive voltages (V_{GS}) were applied onto the two gates. In the meantime, external voltages were added between source and drain (V_{DS}). With increasing V_{DS}, the currents between the source and the drain (I_{DS}) are going through the linear region and the saturation region. The width of the depletion region increases with increasing the reverse bias V_{GS}, thus extends into the channel, further increasing the channel resistance and shrinking the channel width.

The conductivity of JFET carrier-transport channel is modified by the electric field associated with the depletion region of a reverse-biased junction extended into the channel. The capability of the channel to carry currents is the highest when the control junction has zero bias and decreases with increasing reverse bias, as shown in Fig. 4. Therefore, the polymer JFET, operated at depletion-mode, inherently is a normally-on device, which is turned on with no control exerted, and is turned off

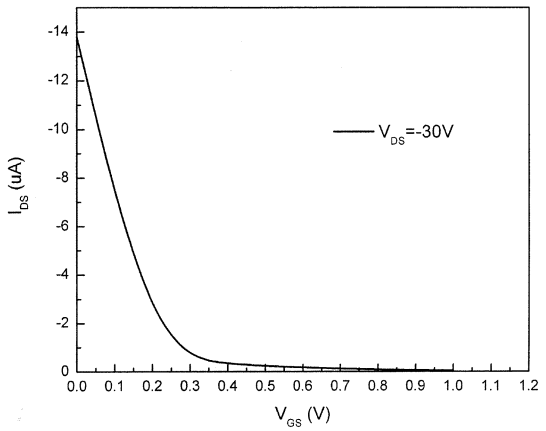

Fig. 5. Transconductance characteristic of a p-channel polymer JFET.

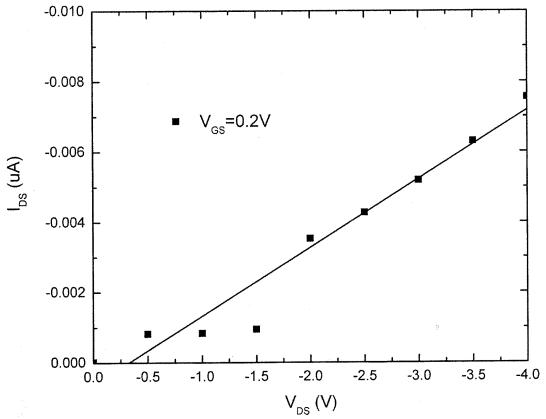

Fig. 6. Drain current at small drain voltage showing the linear relationship.

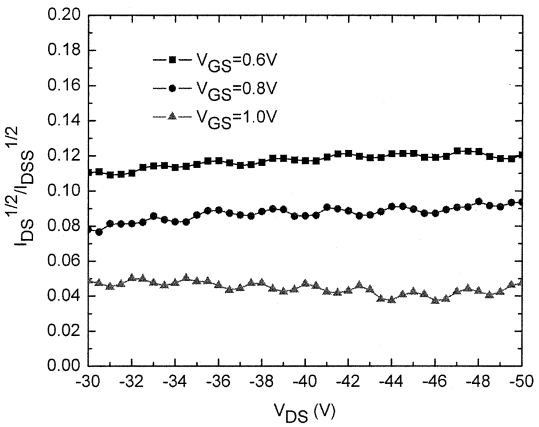

Fig. 7. Showing I_{DS} independent of V_{DS} at saturation region.

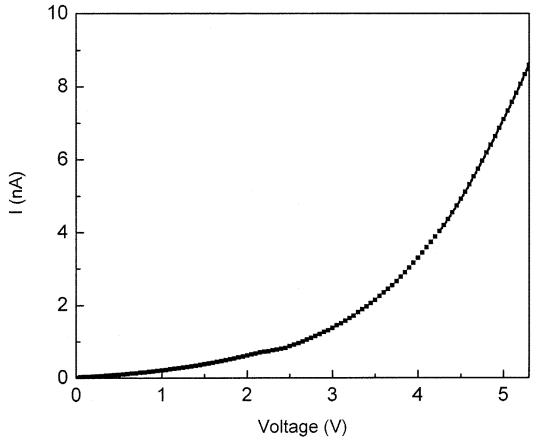

Fig. 8. Forward-biased I–V curve of the junction.

with increasing reverse bias. The transconductance characteristic was plotted in Fig. 5.

In the linear region, we can obtain the relationship among I_{DS}, V_{DS} and V_{GS} as

$$I_{DS} = G_0 \left(1 - \sqrt{\frac{\psi_0 - V_{GS}}{V_{PO}}}\right) V_{DS}. \tag{1}$$

Here, G_0 is the channel conductance without any depletion layers, ψ_0 is the built-in potential, and V_{PO} is the sum of the pinch off voltage V_P and the ψ_0.

$$G_0 = \frac{2qaWu_pN_a}{L}. \tag{2}$$

L is the channel length, W is the channel width, and a is the half of the channel height. The drain current is proportional to the drain voltage at small V_{DS} as shown in Fig. 6.

From the (1), we know the slope is K

$$K = G_0 \left(1 - \sqrt{\frac{\psi_0 - V_{GS}}{V_{PO}}}\right) = \frac{2qaWu_pN_a}{L} \left(1 - \sqrt{\frac{\psi_0 - V_{GS}}{V_{PO}}}\right) \tag{3}$$

which is a parameter relating to the mobility of the conducting polymer channel if the dimension and the material were set.

In the saturation region, the relationship between I_{DS} and V_{GS} can be expressed as

$$I_{DS} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{4}$$

where V_P is the pinch-off voltage, and I_{DSS} denotes the drain saturation current at zero gate voltage. I_{DSS} was 13.8 μA from testing when V_{GS} is 0 V. From the drain testing curves and (4), we derived the following Fig. 7, and it shows that the I_{DS} is independent of the V_{DS}, and it was determined by the V_{GS}. Also, we can obtain the V_P values at each V_{GS} condition.

B. pn–junction

To identify the pn–junction at the gate region, the current–voltage (I–V) characteristics of the gate junction was tested, as shown in Figs. 8 and 9. The breakdown voltage and rectification ratio of the PEDT/PSS/CNPPV junction diode are about 10 V and 2.89, respectively.

C. Al/PEDT/PSS Interface

It has been reported that the Al and the PEDT/PSS can form a Schottky diode. [15] Here, we test the interface of Al and PEDT/PSS, and found that it has the diode feature, as shown

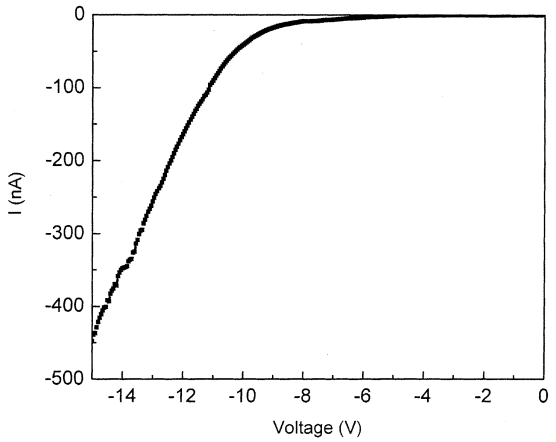

Fig. 9. Reverse-biased I–V curve of the junction.

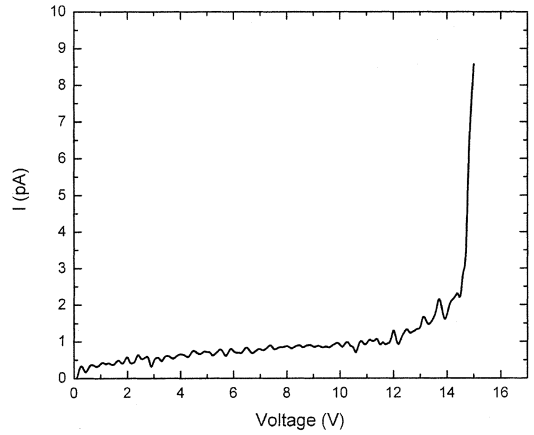

Fig. 10. Forward bias of Al/PEDT/PSS interface.

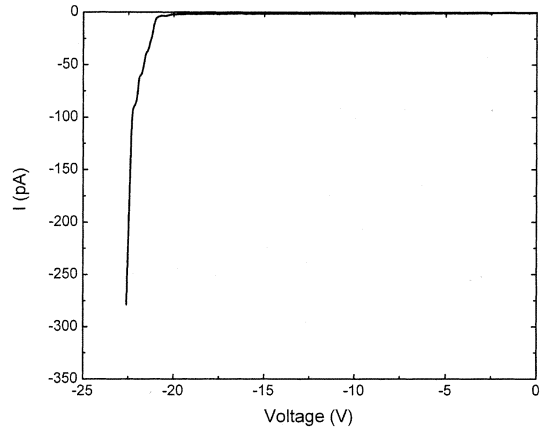

Fig. 11. Reverse bias of Al/PEDT/PSS interface.

in Figs. 10 and 11 for forward and reverse biasing. The breakdown voltage and rectification ratio of the Al/PEDT/PSS junction diode are about 22 V and 3.1, respectively.

D. Polymer JFET and Conventional JFET

Polymer electronic devices are currently in their infancy, like semiconductor devices when they first appeared. As a result, the current performance of these devices is hard comparable to the state-of-the-art semiconductor devices. Though it is difficult to make a comparison, we still found some similarities and differences between these two JFETs, which were listed in Table II.

TABLE II
COMPARISONS BETWEEN POLYMER JFET AND INORGANIC JFET.

		Polymer-JFET	Inorganic JFET
Similarity		working mechanism	
		analyzing methods	
		Polymer works in depletion-mode	
Difference	Fabrication	UV lithography (Experimental stage)	The state-of-the-art industry fabrication
	Structure	Vertical structure	Lateral structure
	Materials	Conducting polymers	Inorganic semiconductors, such GaAs
	Performance	Needs to further improved with the immerging of novel polymer materials	Good.
	Applications	Follower circuit in the experiment stage. No commercial products.	Commercial products. High speed, high power circuits.

Perhaps, with the improvement in polymer materials' properties, such as conductivity and mobility, the performance of the polymer microelectronics devices could compete with the conventional ones.

IV. CONCLUSION

A p-channel polymeric JFET fabricated with UV lithography techniques was realized successfully. The conducting polymer as an active semiconducting component in this microelectronic device behaves in the similar fashion as the inorganic semiconductor counterpart. The operation mechanism of the p-channel polymer JFET was discussed and explained in detail. Furthermore, several important parameters were presented in this paper. Its pinch-off voltage reaches 1 V that is in the applicable range, and the current is $-13.8\ \mu$A at zero gate bias. This work opens a new way to realize JFET, a three-dimensional polymer microelectronic device, with the broad applications such as switches, amplifiers, etc.

REFERENCES

[1] E. Smela *et al.*, "Electrochemical driven polypyrrole bilayers for moving and positioning bulk micromachined silicon plates," *IEEE J. Microelectromech. Syst.*, vol. 8, pp. 373–383, 1999.
[2] ——, "Microfabricating conjugated polymer actuators," *J. Micromech. Microeng.*, vol. 9, pp. 1–18, 1999.
[3] W. H. Edwin *et al.*, "Microfabrication of PPy microactuators and other conjugated polymer devices," *Science*, vol. 290, pp. 1540–1545, 2000.
[4] J. D. Madden *et al.*, "Fabrication by electrodeposition: Building 3D structures&polymer actuators," in *Proc. Sixth Int. Symp. on Micro Machine and Human Science*, 1995, pp. 77–81.
[5] T. A. Skotheim *et al.*, *Handbook of Conducting Polymers*. New York: Marcel Dekker, 1998.
[6] F. Ebisawa, T. Kurokawa, and S. Nara, "Electrical properties of polyacetylene/ polysiloxane interface," *J. Appl. Phys*, vol. 54, pp. 3255–3259, 1983.
[7] T. Kawase *et al.*, "All-polymer thin film transistors fabricated by high-resolution ink-jet printing," in *IEDM Tech. Dig.*, 2000, pp. 623–626.
[8] Y. Liu, T. Cui, and K. Varahramyan, "Fabrication and characteristics of polymeric thin-film capacitor," *Solid State Electron.*, vol. 47, pp. 811–814, 2003.
[9] A. Lodha and R. Singh, "Prospects of manufacturing organic semiconductor-based integation circuits," *IEEE Trans. Semiconduct. Manufact.*, vol. 14, pp. 281–296, 2001.
[10] J. H. Burroughes *et al.*, "New semiconductor device physics in polymer diode and transistor," *Nature*, vol. 335, pp. 137–141, 1988.
[11] C. D. Sheraw *et al.*, "Fast organic circuit on flexible polymeric substrates," in *IEDM Tech. Dig.*, 2000, pp. 619–622.

[12] R. H. Friend *et al.*, "Electroluminescence in conjugated polymers," *Nature*, vol. 397, pp. 121–128, 1999.
[13] D. Braun and A. J. Heeger, "Visible light emission from semiconducting polymer diodes," *Appl. Phys. Lett.*, vol. 58, no. 18, pp. 1982–1984 , 1991.
[14] S. C. Huang *et al.*, "Polyaniline capacitors," *Synth. Metals*, vol. 55–57, pp. 4047–4052, 1993.
[15] G. Liang, T. Cui , and K. Varahramyan, "Fabrication and electrical characteristics of polymer-based Schottky diode," *Solid State Electron.*, vol. 47, pp. 691–694, 2003.

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