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SOI wafer mold with high-aspect-ratio microstructures for hot embossing process

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Abstract This paper reports using a Silicon oil insulator (SOI) wafer as a mold insert for the hot embossing process on high-aspect-ratio microstructures to overcome two drawbacks of Inductive Coupled Etching (ICP) process, the area dependent etching and the micrograss. A thin sacrificial wall to eliminate the undercut in the big open area during ICP etching is also described. A good result of final embossed structure on PMMA with aspect ratio of 12 : 1, uniform thickness, and smooth surface is presented.

1
Introduction

Hot embossing techniques have gained increasing interest as they enable low-cost replication of microstructures with high aspect ratio as well as nm-scale patterns in large area on polymers [1, 2]. On one hand polymers as the raw materials are inexpensive. On the other hand it is an easy way of micromanufacturing, while a complex micromachining step is only necessary once.

Hot embossing exploits the difference in the thermomechanical properties of the hard mold insert and the thermoplastic material. In the first step, a mold insert is fabricated. Next, the mold insert and the polymer substrate are mounted into the , and are heated separately to a temperature above the glass transition temperature of the substrate material. The mold insert is pressed into the substrate with a controlled force. Afterwards, the mold insert are cooled below the glass transition temperature. The polymer material solidifies again, and the tool can be taken out of the embossed microstructure.

For the microstructures with a very high aspect ratio, a metal mold insert was fabricated using LIGA technique in early days. Now, silicon mold inserts fabricated by ICP process is preferred. On one hand, nowadays ICP process can obtain an aspect ratio up to 40 : 1. This is enough for most applications. On the other hand, silicon molds have advantages such as fast and low-cost fabrication, flat surfaces, and suitable hardness, strength, and thermal conductivity [3]. Metal molds fabricated by LIGA technique need an expensive X-ray lithography system and a slow electroplating process. Electroplated nickel molds also have several other disadvantages such as prone to abrasion and wear, voids formed in high-aspect-ratio microstructures, etc.

However, in practice we found that ICP process also has its drawbacks. The two main drawbacks are area dependent etching (also called RIE lag) and micrograss. This paper presents an approach to overcome the two drawbacks through the fabrication of SOI molds, and demonstrates the embossed high-aspect-ratio microstructures on PMMA successfully.

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2
Drawbacks of ICP process

2.1
Area dependent etching

Area dependent etching means that the etching depth is different from different open areas on a silicon wafer in the same process. In another word, the etching rate is faster for the wider trench than the narrower trench as shown in Fig. 1. The main reason is that the exchange rate of the reactive ions for etching silicon at the wider trench bottom is faster than at the narrower trench bottom [4].

Another area dependent etching phenomena is that the profiles of the side walls are different between the narrower trench and the wider open area. In our practice, the side walls in big open area normally get undercut, while the narrow trenches get vertical profiles, as shown in Fig. 2. The main reason for the undercut in the big open area is that the silicon wafer is often negative charged by electrons. The incoming positive ions will be deflected towards the sidewall by the static electrical force. In the narrower trench, the negative potentials on the two closed sidewalls will be counteracted [4].

The first area dependent etching phenomena will result in uneven heights on the final polymer microstructures, the lager thickness for the larger open areas. This will further result in the difficulties either in design phase or in the following processes.

The undercut in the big open area will cause problems, such as silicon mold cracking or rough PMMA side walls, in the demolding process.

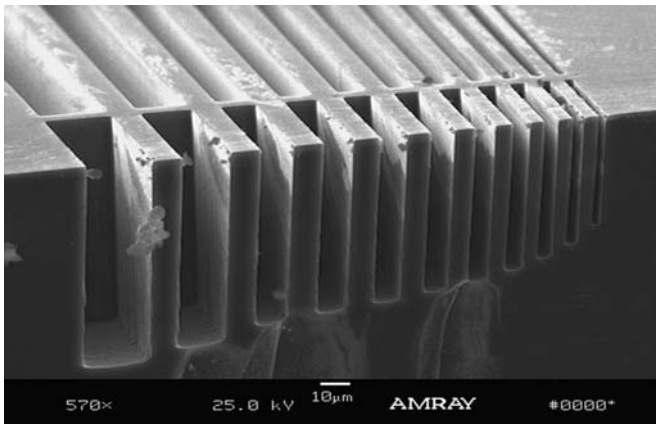

Fig. 1. Area dependent etching

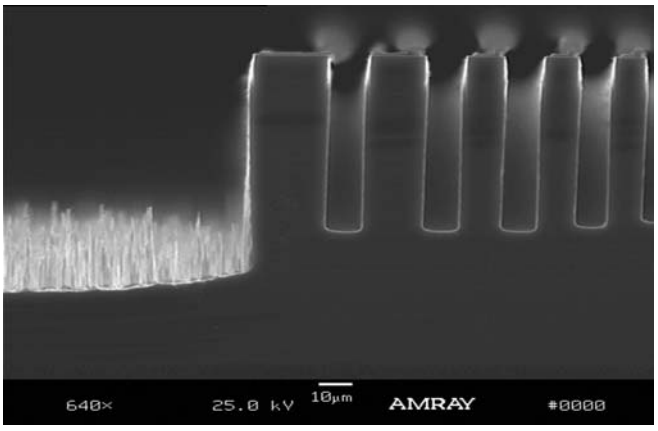

Fig. 3. Micrograss at the bottom of big open areas

2.2 Micrograss

Micrograss often occurs at bottom of the etched big open areas. In an ICP process, there is the C_xF_y polymer deposition phase as well as the etching phase. Micro masks could be formed in the deposition phase. In addition, micro masks could be also formed by masking material redeposition [5]. The energetic reactive ions are highly collimated. The energetic ions can not strike on the silicon surface underneath the micro masks leaving them un-etched. Finally this un-etched silicon will become the micrograss, as shown in Fig. 3.

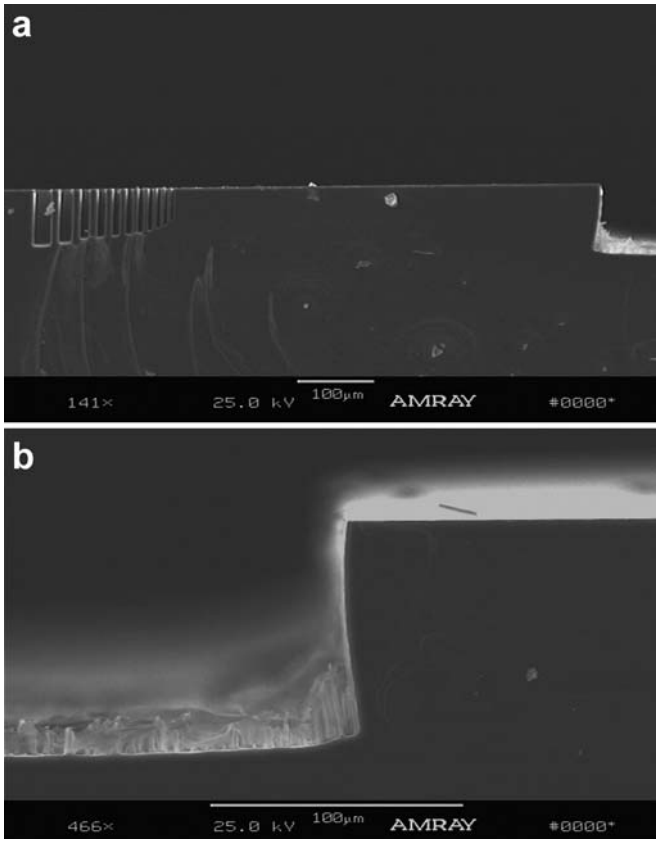

Fig. 2a,b. Undercut in the big open area while the smaller trenches are vertical

This micrograss could result in not only the coarse surface on embossed polymer structures but also the failure of the demolding process.

3 SOI wafer as a mold insert

To overcome these problems from the ICP process, we fabricated the mold insert on a SOI wafer. The SOI wafer has the multi-layer structure as $Si/SiO_2/Si$ of 60/2/400 um. Our final experimental device is a displacement sensor based on the electron tunneling principle. Its key part is a lateral driven comb drive. The key dimensions are: (a) the initial distance between tunneling tip and its counterpart electrode which is also the movable beam of the comb drive is 5 um. This makes the aspect ratio of our device of 12 : 1. (b) the finger width and the gaps between fingers of the comb drive are both 10 um.

The ICP system is Alcatel A-601 from Alcatel Vacuum Technology, France. The SF_6/C_4F_8 gas system is used. The process pressure is 20 mTorr. The DC bias is about 50 V. The wafer is cooled by 20 °C helium from back side. The etching rate is about 4 µm/min. A SOI wafer is over etched for about 2 min to remove the micrograss on the bottom. A good result is shown in Fig. 4. Figure 4a shows the uniform thickness and the smooth bottom by ICP etching on a SOI wafer. As shown in Fig. 4b, the dark lines at the bottom close to the side walls in big open areas indicates the positions of the thin assistant walls, which are already etched off by the end of the ICP process.

However, using a SOI wafer still can not eliminate the undercut in the big open areas. This problem is solved by optimum mask design. An assistant thin wall is added close to the side wall of the big area. The distance between the thin wall and the side wall of big open area is tens of microns so that a vertical trench could be fabricated. The width of this assistant thin wall is decided by the total undercut. The best case is to etch the assistant wall totally through at the bottom by the end of the etching process. Even if there are several microns left at the bottom, this assistant wall will be easily removed by hot embossing during the first time due to the undercut. In our experiment, the width of the assistant wall is 4 µm. This method is illustrated in Fig. 5.

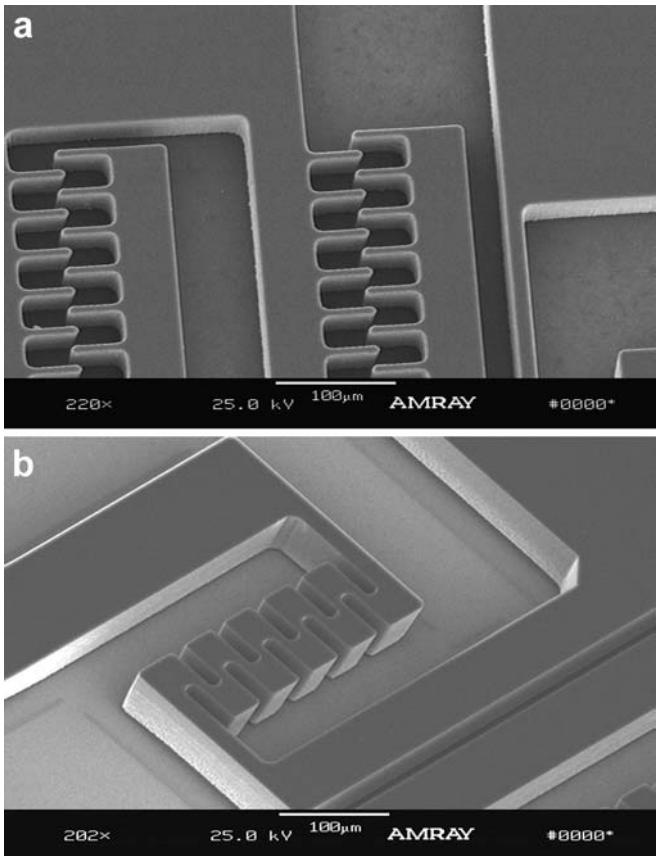

Fig. 4. **a** Even in thickness and smooth at the bottom by ICP etching on a SOI wafer **b** ICP etching with assistant walls

4 Conclusions

A SOI wafer can be used to effectively overcome the drawbacks, area dependent etching and micrograss, of ICP etching process. With a SOI wafer, a mold insert with an even thickness and a smooth surface at the trench bottom has been fabricated successfully. In addition, with a SOI wafer an accurate thickness can be obtained without the precise control of the exact time and the etching rate in the ICP process due to the self-stop characteristic.

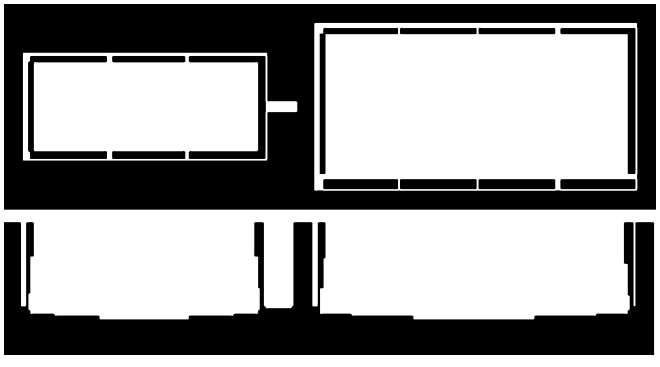

Fig. 5. Schematic of assistant walls to compensate the undercut in big open areas

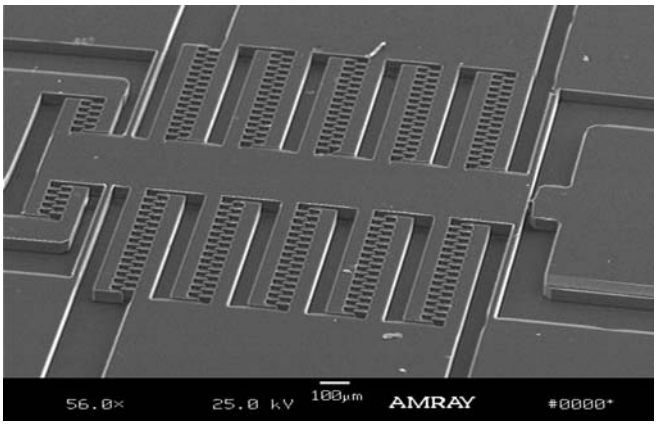

Fig. 6. A good result on PMMA by hot embossing using a SOI mold insert

An assistant wall is an effective method to eliminate the undercut in the big open area. A final structure on PMMA by hot embossing with SOI mold insert is shown in Fig. 6. The detailed process of hot embossing is reported in another paper [6].

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