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Fabrication and characterization of poly(3,4-ethylenedioxythiophene) field-effect transistors

Guirong Liang, Tianhong Cui *

Institute for Micromanufacturing, Louisiana Tech University, 911 Hergot Avenue, P.O. Box 10137, Ruston, LA 71272, USA

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Abstract

The organic field-effect transistors with poly(styrenesulfonate)-doped poly(3,4-ethylenedioxythiophene) (PEDT/PSS) as p-type semiconductor are fabricated on heavily doped silicon substrate working as the gate. Dielectric layer, semiconductor, and source/drain layer are deposited by spin coating and then patterned with UV lithography and RIE techniques using aluminum thin film as the mask. The electrical characteristics of the device have been investigated in the atmosphere at room temperature. The devices have field-effect mobility as high as 0.8 $cm^2/V\,S$, on/off current ratio larger than 10^5, threshold voltage of 9.3 V, and subthreshold slope of 4.5 V/decade.

Keywords: Organic field-effect transistor; Poly(3,4-ethylenedioxythiophene); Spin coating; Reactive ion etching

1. Introduction

Organic field-effect transistors (OFETs) based on semiconductive polymers have attracted increasing interest for the promising applications to flexible, low cost and large area displays, and low-end electronic devices like smart cards due to the extraordinary electrical and mechanical properties of the polymers. A lot of undoped or doped conjugated polymer such as polyaniline [1], polythiophene [2], poly-3-hexyl-thiophene [3], arylamino-poly-(phenylene-vinylene) [4], and alpha-sexithiophene [5] have been demonstrated as the active materials for the OFETs. And since the organic FETs are generally used for low-cost applications, the easy fabrication processes and the simplified structures are of much interest.

In this paper, the fabrication procedure and electrical characteristics of a FET using poly(styrenesulfonate)-doped poly(3,4-ethylenedioxythiophene) (PEDT/PSS) as semiconductor prepared by low-cost spin coating technique are presented. The device requires only three spin coatings and twice photolithography plus reactive ion etching (RIE).

2. Experimental

PEDT/PSS is a kind of promising polymer for electronic applications because it is solution processable and has the transparent property with light and dark blue color when it is dried [6].

The schematic cross-section view of the fabricated FET is shown in Fig. 1. For the fabrication of PEDT/PSS FETs, an n-type heavily doped silicon wafer with resistivity of about 0.01 Ω cm was used as the substrate and the gate electrode for convenience. Poly(4-vinylphenol) (PVP) as the gate dielectric layer was spun on the substrate after wafer cleaning. The thickness of PVP layer was 800 nm. Then the wafer was cured on the hot plate at 110 °C for 5 min to remove the solvent in the thin film. After baking PVP, PEDT/PSS and polypyrrole (PPy working as source/drain electrodes) were deposited by spin coating in sequence. The sample was cured at 115 °C for 5 min after each spin coating. The thickness of PEDT/PSS semiconductor layer was 1 μm as measured.

* Corresponding author. Tel.: +1-318-257-5122; fax: +1-318-257-5104.
E-mail address: tcui@coes.latech.edu (T. Cui).

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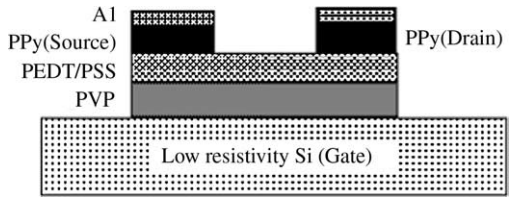

Fig. 1. Schematic structure of FET with PEDT/PSS as the semiconductor.

Here, a layer of aluminum 120 nm thick was thermally evaporated as the pattern mask for RIE process. In our work, two reactive ion etching steps were utilized to pattern the polymer layer. Finally, the PEDT/PSS FETs were implemented with the wet etching for aluminum layer and the RIE etching for polymer layers. The first aluminum wet etching and RIE are used to pattern the whole device structure. And the following Al wet etching forms the source and drain mask for the second RIE etching of PPy to obtain the final device as shown in Fig. 1. The electrical characteristics of the fabricated FET were measured with Keithley SMU236 and 237 in the atmosphere at room temperature.

3. Results and discussion

For the FET described above, the I_D–V_{DS} drain characteristics of a typical FET fabricated with the PEDT/PSS as semiconductor and the PPy as source and drain materials are shown in Fig. 2. This device has a channel length and width of 40 and 300 μm, respectively, and a gate dielectric thickness of 800 nm. In the polymer-based FETs, the I_D is controlled by the V_G applied to the low-resistivity Si. The negative gate voltages enlarge the conduction channel due to the formation of the hole accumulation layer.

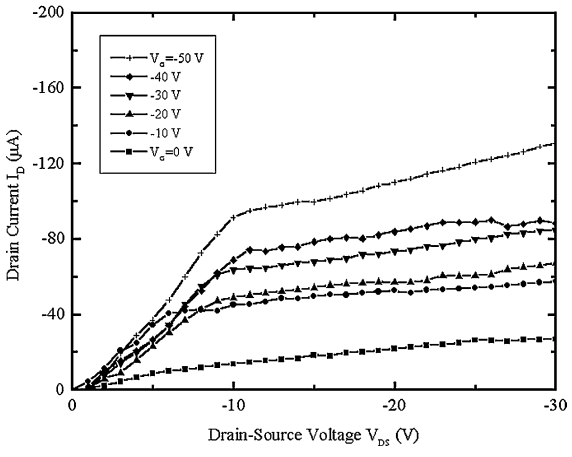

Fig. 2. Typical drain characteristics of OFET with PEDT/PSS as the semiconductor, PVP as the gate dielectric, a heavily doped Si as the gate, a channel length and width of 40 and 300 μm, respectively.

From the Fig. 2, it is found when V_G is at zero volts bias, the current between drain and source, I_D increases linearly with drain–source voltage, V_{DS}. However, when the applied V_G is more negative, I_D rises more sharply at the small V_{DS} and shows a tendency to saturate at relative high drain–source voltage. Thus, the characteristics of FET have two working regions: linear region and saturated region, as shown in Fig. 2. It indicates the channel conductivity is increased with the negative gate voltage. From the Fig. 2, it also shows that the PEDT/PSS works as a p-type organic semiconductor with the holes as the majority carriers. When the negative bias is applied to the gate electrode, the holes are attracted to the region near the dielectric layer between drain and source. Under this bias condition, the conductivity of the channel between drain and source is increased. Thus, the field effect of this FET is due to the accumulation of the holes in the PEDT/PSS film near the PVP gate dielectric layer between drain and source.

To analyze the electrical characteristics of organic FET, we assume that the MOS theory for the traditional Si FETs is still held. Thus, similar to the conventional FETs, the drain current in the linear region and the saturation region can be expressed as [7]:

$$I_D = \frac{W\mu_{FET}C_i}{L} V_{DS}(V_G - V_{th}) \quad (1)$$

$$I_{D\,sat} = \frac{W\mu_{FET}C_i}{2L}(V_G - V_{th})^2 \quad (2)$$

where W and L are the channel width and length, respectively, μ_{FET} is the carrier mobility of the holes in the PEDT/PSS channel, $C_i = \varepsilon_i/d_i$ is the gate dielectric capacitance per unit area (ε_i and d_i are the dielectric constant and the film thickness of the gate dielectric layer, respectively), and V_G, V_{DS}, V_{th} are the gate voltage, drain–source voltage and threshold voltage, respectively.

Fig. 3 shows the measured $I_D^{1/2}$ versus V_G ($= V_{DS}$) characteristics of the PEDT/PSS based FETs. By linearly extrapolating the curve to the V_G axis, the threshold voltage, V_{th} is found to be 9.3 V. This indicates that the FET is a normally-on transistor and the positive gate voltage is necessary to turn off the device. And the hole mobility μ_{FET} can be calculated to be 0.803 $cm^2/V\,S$ from Eq. (2) and Fig. 3. To be useful, the organic FETs must have a sufficiently large on current and low off current for the practical applications, such as to charge the pixel capacitance of the display. When the V_{DS} of −8 V is applied and the gate voltage is swept from 20 to −50 V, the current on/off ratio is about 1.05×10^5 and the subthreshold slope is about 4.5 V/decade.

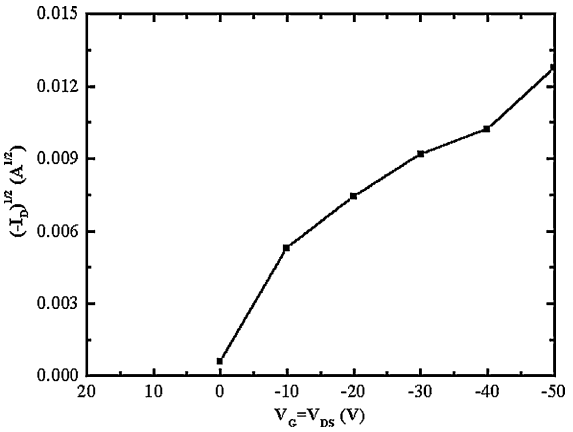

Fig. 3. Plot of $I_D^{1/2}$ vs. V_G $(= V_{DS})$ of OFET comprising a PEDT/PSS as the semiconductor, PVP as the gate dielectric, a heavily doped Si as the gate, a channel length and width of 40 and 300 μm, respectively.

The charge transport in the semiconductive polymer is strongly affected by the doping concentration. The carrier mobility and the conductivity will be changed with the doping. The resistivity of the PEDT/PSS films in this work, as measured by Keithley 236 instrument using two parallel Au electrodes, was found to be 1.26 Ω cm. Thus, from the equation $\sigma = q\mu p$ (q is the elementary electron charge), the carrier concentration, p, can be calculated to be 6.2×10^{18} cm^{-3}, approximately equal to the doping concentration of PEDT/PSS film.

4. Conclusions

In summary, OFETs with the simplified structure have been fabricated with PEDT/PSS as the semiconductor by easy fabrication processes of spin coating and reactive ion etching with aluminum as the pattern mask. By replacing the heavily doped Si with the conductive polymer as the gate, the described fabrication processes may be a potentially low-cost method to fabricate the all-organic field-effect transistors. The fabricated OFETs were characterized in the atmosphere at room temperature, with field-effect mobility as high as 0.8 cm^2/V S, on/off current ratio larger than 10^5, threshold voltage of 9.3 V, and subthreshold slope of 4.5 V/decade. The carrier concentration of the PEDT/PSS film was calculated to be about 6.2×10^{18} cm^{-3}.

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