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Fabrication and characterization of metal–oxide–semiconductor capacitor based on layer-by-layer self-assembled thin films

F Hua, J Shi, Y Lvov and T Cui

Institute for Micromanufacturing, Louisiana Tech University, Ruston, LA 71272, USA

E-mail: tcui@coes.latech.edu

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Abstract
Metal–oxide–semiconductor-capacitor arrays are fabricated on both P and N type silicon wafers using layer-by-layer (LbL) self-assembled insulating layers. The vertical dimension of the self-assembled thin film can be precisely controlled as well as the molecular order. Unlike the conventional process, the LbL self-assembly allows one to obtain the thin films for a semiconductor device with a dramatically lower temperature, lower cost and shorter processing time. The deposited thin film is stable and can grow on any substrate other than silicon. The conventional lithographic technique is employed to pattern the self-assembled thin films, resulting in an extremely high reproducibility. This enables the possibility of industrial applications to fabricate devices with this simplified and versatile technique. A CCD camera was used to produce the image of the pattern, and a white light interferometric microscope was used to measure the dimension and surface roughness of the produced device. The quartz crystal microbalance served to monitor the growth of the self-assembled thin films.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Nanoparticles (NPs) are exciting materials because they exhibit unique electronic, catalytic and optical properties, sometimes different from those of the same bulk material [1, 2]. A great deal of attention has been attracted for applications of NPs as building blocks to microelectronics, optoelectronics and catalysis [3–8].

The relatively new layer-by-layer (LbL) self-assembly, based on alternate adsorption of oppositely charged components (polymers, NPs or proteins), is becoming an increasingly popular technique [9, 10]. At the beginning of the process, three layers of linear polyions are adsorbed onto the substrate to make the surface uniformly charged. Next, negatively charged nanoparticle layers are assembled step by step in alternation with an oppositely charged polycation solution [11–14].

In addition to the thin film deposition, an approach must be developed to readily generate complex and distinct patterns on the LbL self-assembled multilayer films. In our early reports [15, 16], two methods, based on the combination of traditional lithography and LbL assembly, were presented to pattern nanoparticle films. One is referred to by the authors as the 'modified lift-off'. In our experiment, the capacitor arrays were patterned by the 'modified lift-off' as illustrated in figure 1. A layer of photoresist is patterned on silicon wafer in accordance with the geometry of the capacitor and the 'mould' is filled with the NPs. The photoresist is finally dissolved, leaving the NPs that are in the pits. During the lift-off, an ultrasonic wave is introduced to break off the polyions sandwiched between nanoparticle films so that a clear pattern is obtained.

These capacitors can be fabricated onto integrated circuit chips. Metal–oxide–semiconductor (MOS) capacitors, with

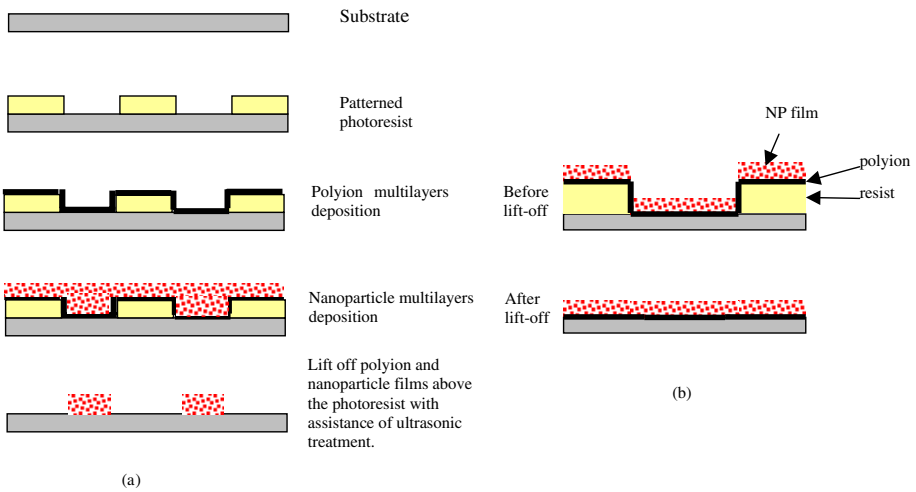

Figure 1. (a) Scheme of patterning nanoparticle thin films with ultrasonic treatment (modified lift-off). (b) Scheme of patterning nanoparticle thin films without ultrasonic treatment (conventional lift-off). NP and polyion films cannot be lifted off because the linkages between polyion molecules are not disconnected.

thermal SiO_2 as the gate oxide, have become the prime structure to carry out digital functions in silicon integrated circuits. However, the fabrication of a MOS capacitor using the conventional silicon MOS technology demands sophisticated facilities. High process temperature also needs to be balanced to avoid the damage to subsequent processes, and the growth rate of the thermal silicon dioxide is usually very low. Hereby, an approach to fabricate the basic MOS capacitor with a technique combining traditional lithographic technique and LbL self-assembly was developed because a dielectric layer consisting of silica and polyion can be self-assembled easily and rapidly. The insulating layer is made of six layers of LbL self-assembled silica nanoparticle thin film. Capacitors are fabricated on 4 inch P-type and N-type silicon wafers. The measured capacitance–voltage (C–V) curves are in compliance with typical MOS capacitors. Compared to the traditional process, this has the advantages of low temperature, low cost and short processing time. LbL self-assembly is also called molecular beaker epitaxy because it just requires several beakers to realize the 'dipping in' adsorption. The lithographic technique is already a mature process, widely used in the microelectronic industry. The combination of traditional lithography and LbL self-assembly guarantees an extremely high reproducibility in the fabrication of semiconductor devices. The regular dipping also enables the automation of this process if it is applied to mass production. The self-assembled thin film of silica nanoparticle is stable enough to withstand the ultrasonic wave. The simplicity and reliability of this process to fabricate a simple MOS capacitor provides a new way to fabricate other microelectronic or optoelectronic devices by traditional lithography and LbL self-assembled building blocks.

2. Experimental methods

2.1. Materials

Poly(diallyldimethylammonium chloride), MW 200–300 K (PDDA, Aldrich), and sodium poly(styrenesulfonate), MW 70 000 (PSS, Aldrich), were commercially available and used without further purification at a concentration of 1.5–3 mg ml^{-1}. The pH of the solutions was adjusted by adding aqueous NaOH or HCl. PDDA is a quarternary ammonium linear polycation and PSS (pK_a 1) is a linear polyanion. Polyions were used in solutions at pH 8. SiO_2 colloidal solutions (231 mg ml^{-1}, Nissan Chemical) were diluted in water to provide concentrations of 10 mg ml^{-1} at pH 9. The diameter of the silica particles was 45 ± 5 nm.

2.2. Quartz crystal microbalance (QCM) technique

QCM equipment produced by USI System in Japan was used to monitor the assembly process. The resonators used were covered by evaporated silver electrodes on both sides. The resonance frequency was 9 MHz (AT cut). The QCM resonator was immersed for a given period of time in a polyelectrolyte solution and dried in a nitrogen stream. The frequency changes were then measured. All experiments were carried out in an air-conditioned room at about 22 °C.

A QCM is a microbalance suitable to detect the tiny mass and thickness adsorbed on its face. It senses the resonance frequency directly which results in a high sensitivity. The frequency decrease can be converted to an increment of adsorbed mass and thickness as the following equations by taking into account the characteristics of quartz resonators, so the prefactors are specific to the system.

$$\Delta F\,(\mathrm{Hz}) = -1.83 \times 10^{8}\,(\mathrm{Hz\,cm^2/g})\Delta M(\mathrm{g})/\mathrm{A}\,(\mathrm{cm^2}) \quad (1)$$

where M (g) is the adsorbed mass, ΔF (Hz) is the frequency shift and A is the apparent area of quartz microbalance placed between QCM electrodes. This is 0.16 ± 0.01 cm^2 in our system. Then, one finds that 1 Hz change in ΔF corresponds to 0.9 ng in weight. The thickness of the alternate layer corresponding to QCM frequency shift was determined by observation of the film cross-section from SEM images of cut resonators coated with silicon/polycation films, which gives the following relationship with ±5% error [11]:

$$d\,(\mathrm{nm}) = -0.022\,(\mathrm{nm\,Hz^{-1}})\Delta F\,(\mathrm{Hz}). \quad (2)$$

In the first stage, a well defined precursor film with a thickness of about 10 nm was assembled from PDDA and PSS onto resonators or mica. The precursor films contained three polyion layers in the alternating mode, PDDA/PSS, and the terminal layer was 'positive' PDDA. Then a substrate was alternately immersed for 10 min in aqueous dispersions of SiO_2 and in aqueous PDDA with intermediate water washing. This process was periodically interrupted for the purpose of measuring QCM resonance frequency.

2.3. Scanning electron microscopy

A resonator with an assembled film was cut and coated with 20 Å thick Pt by use of an ion-coater (Hitachi E-1030 ion sputter, 10 mA/10 Pa) under argon atmosphere. Scanning electron micrographs were obtained with a Hitachi S-900 instrument at an acceleration voltage of 25 kV. SEM images of MOS capacitors were made with a lower resolution instrument, 'AMRAY'.

2.4. Micromanufacturing

The substrates were 4 inch silicon wafers, P type (orientation ⟨100⟩, >1Ω cm) and N type (orientation ⟨100⟩, 1–100 Ω cm), from Silicon Quest. A double-sided mask aligner (EV420 from Electronic Visions) was used as the UV light illuminator. Aluminium layers were deposited on a silicon substrate by the DV-502A high vacuum evaporator from Denton Vacuum, Inc. The WYK RST white light interferometer microscope was used to measure the surface roughness and dimension of the thin film. The electronic characteristic instrument was from Keithley Co., Inc. Ultrasonication was performed with an 8892 Cole-Parmer ultrasonic cleaner.

Initially, the 4 inch silicon wafer was put into sulfuric acid and hydrogen peroxide solution (volume ratio 3:7) at 70 °C for 1 h. The wafer was completely rinsed by DI water and baked on a hotplate at 150 °C for 5 min to remove the moisture. Then it was placed on a spinner to coat a layer of negative photoresist (NR9-1500P from Futurrex). The maximum speed was set at 1000 rpm for 40 s. The wafer with photoresist was baked on a hotplate at 150 °C for 80 s. The resist was subsequently exposed by UV light for 22 s to transfer the pattern from the mask onto the resist. Next, it was baked at 100 °C for 80 s and finally immersed in developer solution for 12 s. At this point, the capacitor pattern was transferred onto the resist.

Following the above steps, LbL assembly of 45 nm silica particles was implemented on the silicon wafer. The sequence of the alternate immersion was [PDDA (10 min)+ PSS (10 min)]$_2$ + [PDDA (10 min) + silica (10 min)]$_6$. The intermediate rinsing and drying after each immersion was necessary. The rinsing was done by purging the wafer in DI water flow for 1 min. The wafer was placed on a spinner and spun to remove water by centrifugal force. The maximum rotation speed was set at 1300 rpm for a time of 45 s. Subsequently, the deposition of aluminium was carried out at a pressure of 10–5 mTorr with a deposition rate of 2 Å s^{-1} until a thickness of 3000 Å was reached. The wafer was then soaked into acetone solution for 5 min to dissolve the photoresist, and an ultrasonic bath was introduced for roughly 3 s to improve the lift-off.

The capacitors were made on both P- and N-type wafers. The capacitance versus voltage curves were obtained under a voltage range from −2 to 2 V with a step of 20 mV.

3. Results and discussions

Figure 2(a) shows an SEM image of the (45 nm silica/PDDA)$_4$ multilayer cross-section. The film has a permanent thickness of 170 nm, leading to 43 nm for every bilayer close to the silica particle diameter. A film mass from QCM and film thickness from SEM gives a density of the SiO_2/PDDA multilayers as $\rho = 1.43 \pm 0.05$ g cm^{-3}. To calculate the silica packing coefficient in the films, it is reasonable to assume that the dry film consists of SiO_2, PDDA and air-filled pores. The mass ratio of PDDA to PDDA/SiO_2 bilayer obtained from QCM measurements is 0.08. Given the component densities ($\rho = 1.43$, $\rho_{SiO_2} = 2.2$ and $\rho_{PDDA} = 1.1$ g cm^{-3}), the volume ratio is obtained as $V_{PDDA}/V_{bilayer} = 0.1$. From the equation

$$\rho_{PDDA} V_{PDDA} + \rho_{SiO_2} V_{SiO_2} + \rho_{air} V_{air} = \rho V \qquad (3)$$

where the air term is very small, V_{SiO_2}/V is figured out to be 0.7. This is very close to the theoretical dense-packing coefficient for spheres (0.63), and corresponds to details in the SEM micrographs. The SiO_2/PDDA film volume composition is 70% SiO_2 + 10% polycation +20% air-filled pores. These pores are formed by closely packed 45 nm SiO_2 and have a typical dimension of 15 nm. Therefore, the dielectric constant of our silica/PDDA multilayer is different from silica due to about 30% of inclusions, such as air, polyion layers etc. In the analysis of the MOS devices, it is found that the dielectric constant was slightly higher than the one for thermal silica. In our group, it is possible to produce ultrathin multilayers of silica NPs with thickness ranging from a hundred to hundreds of nanometres with precision of about 10 nm. These films have a porous structure related to the close packing of silica spheres in the layer.

As shown in figure 3, clear patterns of the capacitor arrays with sharp borders were created on a silicon wafer. The arrays consist of round and square capacitors with various sizes. All 45 nm SiO_2 spheres were closely packed to form a dense structure. The surface roughness of the capacitor was 6.5 nm measured by a roughness step tester (RST). The growth step can be easily estimated by measuring the frequency shift of the quartz crystal microbalance resonator, and the monolayer thickness can be calculated accordingly by the Sauerbrey equation. Figure 2(b) gives the QCM monitoring of alternate PDDA and SiO_2 adsorption where the thickness was calculated from frequency shifts with formula 2. As recorded by QCM, at every assembly step, the component monolayer was formed. This shows that, at the last cycle, the thickness of the SiO_2 layers is 260 nm. When added to the 300 nm aluminium electrode, the height of the whole device is 567 nm, well in compliance with the 2D profile of figure 3(b).

The fabricated device demonstrates the C–V curve of a typical MOS capacitor with distinct accumulation, depletion and inversion regions, as shown in figure 4. The MOS structure is basically a capacitor with silica as the dielectric material. If the silicon were a perfect conductor, the parallel-plate capacitance would be determined by the oxide capacitance as

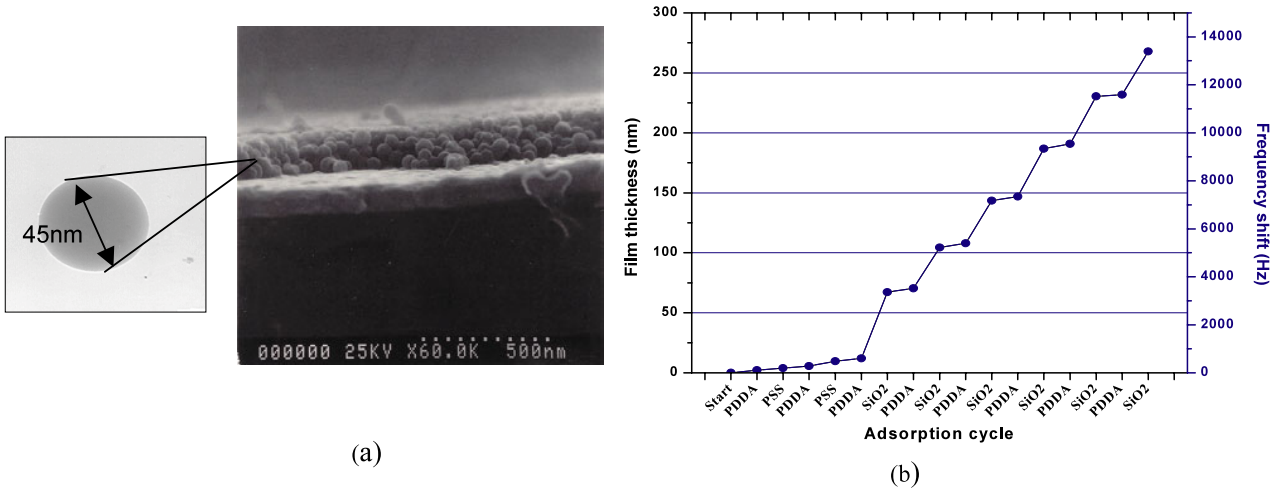

Figure 2. (a) SEM image of cross-section of (45 nm silica/PDDA)$_4$ multilayer on silver electrode; (b) QCM monitored 45 nm silica growth.

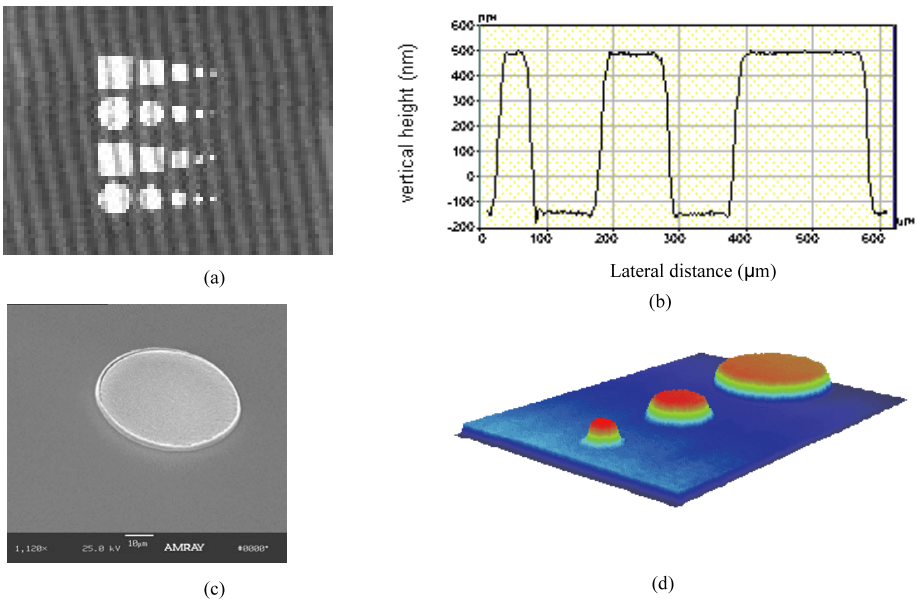

Figure 3. (a) Optical image of the capacitor arrays; the minimum diameter or size is 50 μm; (b) 2D profile; (c) SEM image of layers of 45 nm silica particle thin film; (d) 3D plot of the capacitors.

it is in the accumulation region. However, it always deviates from the oxide capacitance due to the voltage dependence of the surface space-charge layer in silicon. The space charge occurring at the interface of silicon and oxide acts as another capacitance in series with the oxide capacitor, giving an overall capacitance that is smaller than the pure oxide capacitance. Since the inversion of a P-type MOS capacitor happens at a positive voltage and an N-type one at a negative voltage, the C–V curves move in opposite directions for P- and N-type MOS capacitors. If the layer of silicon dioxide were produced by conventional thermal oxidation, the dielectric constant would be 3.9. Given the size of each square device, 200 μm $\times$ 200 μm and 267 nm high, the oxide capacitance is calculated as 5.2 pF, reasonably close to the experimental data, 8 pF. The slightly larger value means a larger dielectric constant of the LbL self-assembled insulator layer. The precursor and intermediate polyion multilayer is the root for the higher dielectric constant because the dielectric constant of the polyion films is normally ten times higher than silica [17]. The experimental results also show that the capacitance of each device is strictly proportional to the area of electrode, implying an extremely high reproducibility of the processes. The leakage current is hardly measurable in the testing system. Another important parameter, the flatband voltage $V_{FB} \approx -0.2$ to -0.5 V, can be extracted from figure 4 by observing the turning point of the depletion and accumulation region.

The process will take about 5.5 h including 1 h of cleaning, 1 h of lithography and 3.5 h of LbL self-assembly. In our process, a conventional lithographic technique, such as lift-off, was used to pattern the capacitors on multilayer films. However, because the LbL self-assembled nanoparticle films are unlike the conventional thin films in many respects, modification and optimization of the traditional process is required.

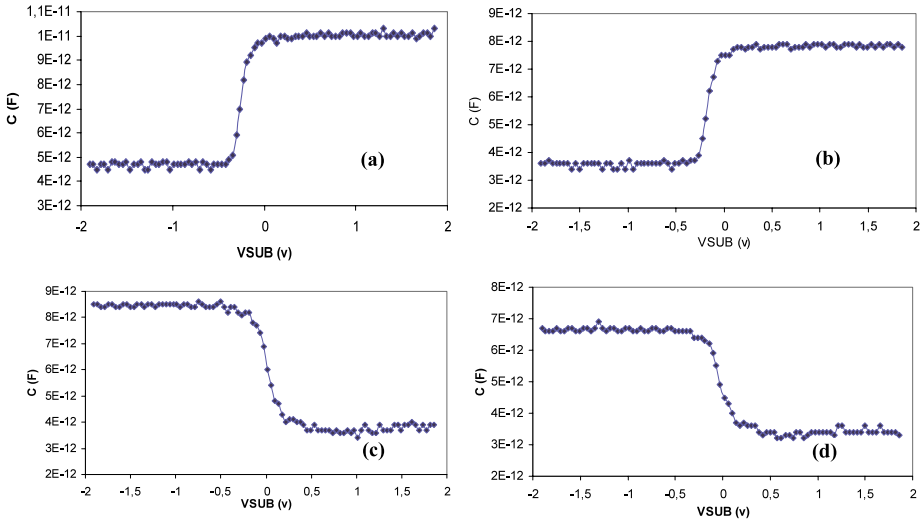

Figure 4. Capacitance versus voltage curves of MOS P- and N-type capacitors: (a) N-type square capacitor with size of 200 μm; (b) N-type round capacitor with diameter of 200 μm; (c) P-type square capacitor with size of 200 μm; (d) P-type round capacitor with diameter of 200 μm.

During the lift-off it was better to introduce ultrasonic treatment for 3 s when the wafer was soaked in developer solution. Inside the structure of the nanoparticle film, polyion multilayers such as PDDA and PSS were sandwiched between the nanoparticle film and photoresist as a kind of 'chemical glue'. The structure of the polyion is like a long thread which strongly links to each other. It is hard to break them up during the lift-off, so in some areas the nanoparticle and polyion multilayer cannot be removed when the photoresist is dissolved. They just drop down and re-attach to the film underneath, as shown in figure 1(b). The ultrasonic treatment is introduced to disconnect the linkage between polyion branches and obtain a more distinct pattern with higher reproducibility.

Other dielectric materials such as montmorillonite had also been tested as the insulating layer. They did not perform as well as the silica nanoparticles although the monolayer thickness can be more precisely controlled. There are many other NPs suitable for LbL self-assembly which may function differently for various devices.

4. Conclusions

LbL self-assembled thin films have been introduced into the fabrication of basic MOS devices. The corresponding patterning technique has also been developed to process the LbL assembled thin film. The resulting geometry and electronic characteristics indicate the extension of this technique to fabricate other semiconductor or optoelectronic devices. The combination of LbL assembly with the mature lithography process offers us the opportunity to fabricate devices rapidly with inexpensive beakers at room temperature. The additive thin films can be coated on almost any material in nature. It also provides a remarkable reliability and possibility of automation for batch production.

A wide array of potential applications exists for the fabrication of conventional devices using nano-bricks, as well as lowering the price and reducing the complexity of the traditional processes. More sophisticated devices such as MOS field effect transistors made by this technique are under investigation.

Acknowledgments

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