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Fabrication of indium resistors by layer-by-layer nanoassembly and microlithography techniques

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Abstract

Layer-by-layer self-assembled thin films made of indium nanoparticles have been investigated as conductive materials to fabricate resistors. The functional resistors degrade as the current passes through the devices. However, it tends to be stable at some acceptable values. The rapid thermal annealing has a significant effect on the electrical characteristics of this thin film. The resistivity before annealing was 2.4×10^5 Ω cm, and it was reduced dramatically after annealing to about 0.9 Ω cm.

Keywords: Layer-by-layer self-assembly; Indium; Resistor; Resistivity

1. Introduction

Recently, technologies for the production of metallic, semiconductive, and insulating nanocrystals are able to provide nanoparticles that function similarly to the high-grade materials used by the modern microelectronics industries [1,2]. Due to their unique properties and versatility, nanoparticles have become the focus of material research for applications to microelectronics, optoelectronics, catalysis, fundamental research in solid state physics [3–5]. Metal nanoparticles and nanostructures have been the subject of many extensive scientific and practical investigations [6–9]. There are a number of applications requiring medium to low resolution lines (10 μm and up) including solar cells, microwave circuits, printed circuited boards, toys, and microelectronic packaging. The optimum deposition approach is the one that minimizes capital investment while reducing ancillary processing. Direct writing of inks to form conductor lines has inherent processing advantages over screen-printing and vapor deposition because no post-printing thermal treatments or photolithographic processing are required. However, they have some special requirements for the ink. These inks must function to produce adherent and electrically connected layers at suitable processing temperatures. In addition, high purity may be required to attain satisfactory conductivity in the deposited layers [10]. Liquid embossing overcomes these limitations through two critical and different approaches compared to other techniques. The first is that the patterned material remain a liquid throughout the embossing, requiring no chemical reaction or phase change to occur during the actual patterning. The second is that the embossing pushes through the thin liquid film and contacts the substrate beneath, enabling the additive fabrication of electrically isolated features and the direct formation of via, both without the etching required for contact-printing and imprint schemes. However, it still depends on the template fabrication [11]. The master is fabricated using microlithography techniques such as photolithography, micromachining, e-beam writing, or from available relief structures such as diffraction gratings [12].

We developed the modified lift-off and the metal mask techniques based on the Layer-by-layer (LbL) self-assembly and the traditional microlithography [13–15]. Self-assembled monolayer or multilayers were utilized to

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generate the devices such as capacitors [16] and field-effect transistors. Because the layer-by-layer self-assembly and the lithography techniques are mature processes and lithography is widely applied to the modern semiconductor industries, the combinative technique will be economical and suitable for mass production. By modifying the traditional processes, the nanostructures composed of nano building blocks can be realized. As the lithography technique is used in the semiconductor industry, the process results in such a high reproducibility that distinct patterns can be created in almost all of the dies on the wafer.

As we all know well, the microelectronic devices consist of conducting layers, insulating layers, and semiconductive layers. For the nanoparticle-based devices, both the semiconductive layer and the insulating layer can be fabricated by LbL self-assembly, while the conducting layers are fabricated by evaporation or sputtering [16]. To our knowledge, no conducting layers were generated by LbL self-assembly with inorganic nanoparticles. In this paper, indium nanoparticles were utilized as the building blocks to obtain conducting lines, especially resistors.

2. Experiments

2.1. Materials and equipment

Materials involved are poly(dimethyldiallyl ammonium chloride) (PDDA) aqueous solution, MW 200 to 300 K, 3 mg/ml, 0.5 M NaCl and sodium poly(styrene-sulfonate) (PSS) aqueous solution, MW 70 K, 3 mg/ml, 0.5 M NaCl. Both of them were obtained from Aldrich Sigma. Dispersion of indium nanoparticles, 0.15 g/ml, 10–80 nm in diameter was also purchased from Aldrich Sigma.

Rapid thermal annealing (RTA) (RTA-600S, Modular Process Technology Corp.) was used in the experiments.

2.2. Methods

A 4-in. silicon wafer was immersed in H_2SO_4 and H_2O_2 solution (volume ratio 7:3) at 70 °C for 1 h. Next, it was "hardbaked" at 115 °C on a hotplate for 5 min. A layer of 1 μm photoresist was spun on the silicon wafer. The speed was 1500 rpm, the ramp was 200 r/s, and the time is 40 s. It was baked on the hotplate at 115 °C for 1 min. It was exposed under UV light for 7 s, and the desired patterns on a photomask were transferred onto the surface of photoresist through development. The developer was MF-319, and time was 40 s.

The substrate was soaked into PDDA, PSS solutions alternatively, in the sequence of PDDA (20 min) + (PSS (10 min) + PDDA (10 min))$_2$ + PSS (10 min). The substrate was rinsed using DI water for 1 min, and dried by spinning between the two alternate immersions. The speed of the spinner was 1300 rpm, the ramp was 300 r/s, and the time is 40 s. Indium nanoparticles were adsorbed alternately with PSS in the sequence of (indium (2.5 min) + PSS (10 min))$_{10}$, and dried by the parallel nitrogen gas flow between the two alternate immersions.

The substrate was put into an acetone solution with ultrasonic treatment for 7 s to remove the photoresist. Finally, the patterned thin film went through Rapid Thermal Annealing at 300 °C for 3 s.

3. Results and discussion

Fig. 1 shows the lift-off method used to fabricate the functional devices and the microscopic configuration of the conducting line. It can work well on the thin film made of indium nanoparticles. The clear image can be seen in Fig. 1(b).

Fig. 2 shows the electrical characteristics of fabricated resistors. The electrical properties were determined by the standard four-probe measurements. From this

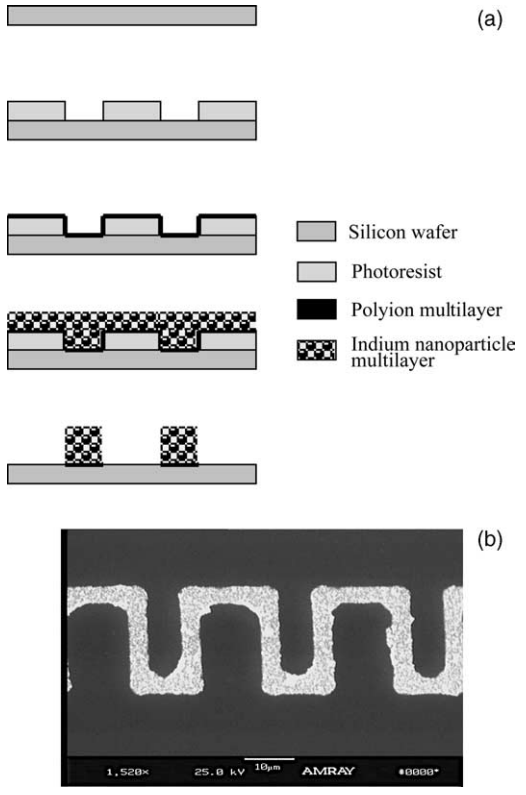

Fig. 1. (a) Scheme of patterning nanoparticle thin films with the lift-off approach and (b) patterned conducting line made of indium nanoparticles (the first six steps are platform layers).

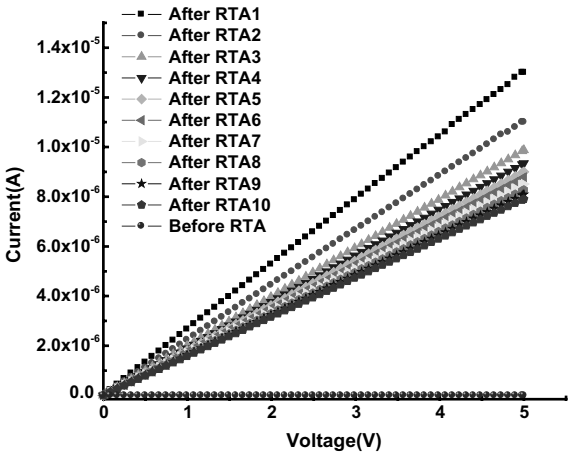

Fig. 2. Typical I–V curves measured on patterned LbL indium nanoparticle thin film (before and after RTA). RTA 1, 2, 3, ... refer to the measuring sequences.

figure, we can see that rapid thermal annealing (RTA) has significant effects on conductance of the fabricated devices. The measurement was taken on the resistors 10 μm wide and 220 μm long. From the results obtained by roughness surface tester (RST), the thickness of the film was around 543 nm. By combining the measured resistance R of the resistor with its geometry, the resistivity ρ of the patterned indium was calculated using the formula $\rho = Rwh/l$, where h, w, and l are the thickness, the width, and the length of the wire made of indium nanoparticles, respectively.

The resistivity before annealing was calculated as 2.4×10^5 Ω cm. It was reduced dramatically after annealing as about 0.9 Ω cm. In the atmosphere, the conductance of the devices decreased. The performance of the resistors degraded as the current went through the devices. This may be caused by the heat generated when the voltages were applied onto the resistors. One of the possible reasons for the conductance decrease is the oxidation of the nanoparticles. Indium can be oxidized to In_2O_3 when it was heated in the air, and thus it will become more insulating. The other possible reason was that water vapor (H_2O) contained in the air may be adsorbed by the multilayer so that the conductance was reduced.

The degradation became less significant as we continued to apply voltage onto the device. At a certain value, it was getting stable. The reason is not very clear yet. It is predicted that only some outside indium nanoparticles can be oxidized. The stable value is reached after the maximum oxidation occurs. Therefore, this device can have relatively consistent functions if the current is kept going through the resistors for a period of time before it is actually operational.

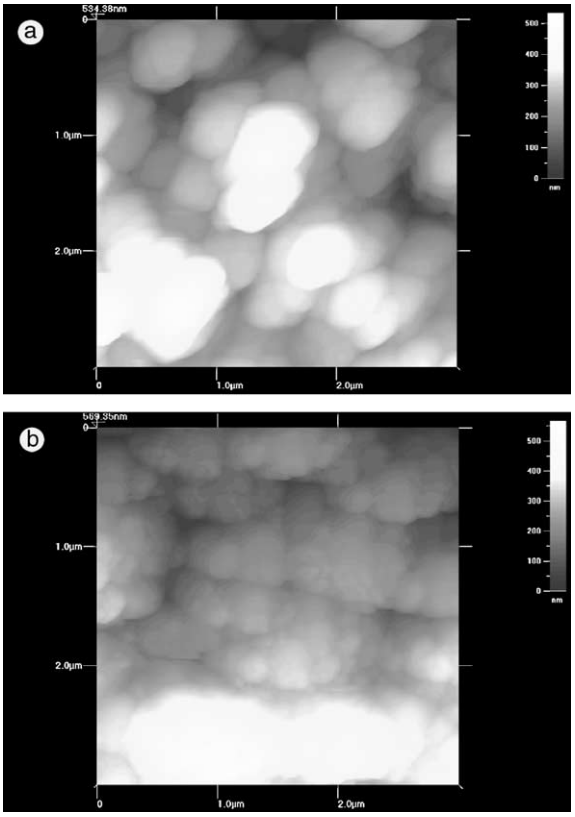

Fig. 3. AFM images taken on the multilayer thin film of indium nanoparticles and polyions: (a) before RTA and (b) after RTA.

Fig. 3 illustrates the two AFM images before and after RTA, respectively. Before annealing, the nanoparticles were separately distributed. They did not contact each other very well. RTA made it possible to form the cluster of indium nanoparticels. The melting point of indium is about 140 °C, and our annealing temperature is about 300 °C. Therefore, when the nanoparticles were heated, they might be melted and aggregated, as shown in Fig. 3(b). The other possible reason is the removal of polyions during the annealing process. RST results show that the thickness of multilayer decreased lightly after annealing.

Several different types of metal nanoparticles were investigated, such as gold, platinum, and copper nanoparticles. All of them have lower resistivity than indium as bulk materials. However, they did not show good conductivities when we tried the same fabrication process on them as we did on the Indium nanoparticles. The possible reason is that all of these materials have much higher melting temperatures, therefore we could not obtain the good contact among nanoparticles as indium nanopartcles even through RTA.

4. Conclusions

Resistors based on multilayer thin films made of indium nanoparticles and polyions were successfully fabricated by the LbL self-assembly and the traditional lithography techniques. It has the lowest resistivity ever realized by the LbL technique, and can work as a conductive layer in the microelectronic devices. Rapid thermal annealing can improve the conductance dramatically. One of the possible reasons is that the aggregation of indium nanoparticles through rapid thermal annealing due to its low melting temperature. Degradation is a problem for this device. However, one can still have relatively good and stable properties by applying voltage onto it for a certain period of time. This device will have the potential applications to microelectronic devices and MEMS with the advantages such as lower cost, simpler processes, etc.

Acknowledgement

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