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We report an approach of wafer-scale addressable single-crystalline graphene (SCG) arrays growth by using pre-patterned seeds to control the nucleation. The growth mechanism and superb properties of SCG were studied. Large array of free-standing SCG devices were realized. Characterization of SCG as nano switches shows excellent performance with life time (>22 000 times) two orders longer than that of other graphene nano switches reported so far. This work not only shows the possibility of producing wafer-scale high quality SCG device arrays but also explores the superb performance of SCG as nano devices. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4894255]

Graphene, a two-dimensional honeycomb crystal of sp^2-bonded carbon atoms, has drawn significant attention in both fundamental and applied research fields, owing to its extraordinary electrical and mechanical properties.[1] Graphene's extremely high carrier mobility[2] and thermal conductivity[3] make it an excellent candidate for next generation electronic applications.[4–8] The high Young's modulus[9] and breaking strength[10] make it an ideal material for nanoelectromechanical systems (NEMS).[11–14] Several techniques have been developed for generating high-quality graphene films.[15–24] Chemical vapor deposition (CVD) with Cu substrate has the ability for the growth of large-area monolayer graphene[18] with relatively low cost, attracting increasing attention.

However, large area graphene films prepared by current growth methods are polycrystalline material with randomly distributed grain boundaries. So, it seems unlikely to get rid of grain boundaries in fabricated graphene devices, especially in the case of device arrays. Due to grain boundaries, most of graphene's electrical and mechanical properties degrade dramatically. Fracture strength of polycrystalline graphene with small mismatch angles at grain boundary is much smaller than that of intrinsic graphene,[25] thus grain boundary is generally believed to have a detrimental effect on graphene based device's performance. Therefore, it is critical to either obtain wafer-size single-crystalline graphene (SCG), or wafer-size addressable SCG grains to avoid the grain boundaries in fabricated devices. Various methods have been reported to increase graphene's grain sizes in CVD process,[26–30] but wafer-scale SCG is still very difficult to realize. Limited experimental work has been directed towards controlling the nucleation of individual graphene grains.[20,31] Nevertheless, their quality is not comparable to intrinsic graphene (graphene has disorder inside the grain which has detrimental effect on film quality[31]), and the growth mechanism from artificial seeds remains unknown. Therefore, large-scale high quality SCG devices have never been achieved. Additionally, CVD graphene NEMS reported so far are polycrystalline.[19,32,33] Broken failure due to weak grain boundary largely prevents their practical applications. Therefore, SCG NEMS is highly desired.

Here, we report a top-down approach with LPCVD (low pressure chemical vapor deposition) to obtain site- and alignment-controllable wafer-scale SCG arrays on copper foil film. SCGs show very good quality. The growth mechanism from artificial seeds and the method to derive SCG with high quality are investigated. Large arrays of free-standing SCG devices on arbitrary substrates integrated with existing semiconductor processes were achieved. Sequentially, we explored the superb performance of SCG as NEMS switches.

SCG growth approach is illustrated in Figure 1(a). First, LPCVD growth of graphene was carried out in a quartz tube furnace at 1050 °C with a mixture of 7.2 sccm methane and 2 sccm hydrogen. After 30 min growth, the copper foil was covered with continuous polycrystalline graphene film (>95% monolayer). Then, patterned graphene seeds of 1 μm in diameter or smaller could be obtained after oxygen plasma etching as shown in Figure 1(b). Finally, precisely addressable SCG flakes were obtained after the second round LPCVD growth, with their sites determined by pre-patterned seed patterns. Increasing the quality of seeds is an effective way to achieve SCG with better quality. Previously reported annealing time before second round growth is too long[20,31] (3 h), so the copper loss may have detrimental effect on the seeds. In our experiment, the annealing time is less than 30 min. During the second round growth, the copper foil with graphene seeds was put into the furnace with its patterned copper surface upside-down so that there would be a small gap (or a tiny "furnace") between the copper foil and the quartz boat. This tiny furnace could reduce copper atoms loss from copper substrate at low pressure and high growth temperature, which can not only protect the seeds but also result in lower nucleation density. A relatively low methane flow rate of 0.12 sccm with hydrogen flow rate of 10 sccm at high temperature of 1050 °C was applied in order to further reduce randomly nucleated grains. The growth duration is 6 min. Additionally, oxygen dry etching can increase O on exposed copper surface, suppressing randomly nucleated grains effectively.[28] In Figure 1(c), randomly nucleated grains are hardly observed. A single SCG flake with star-like shape is shown in Figure 1(d), commonly observed in regular

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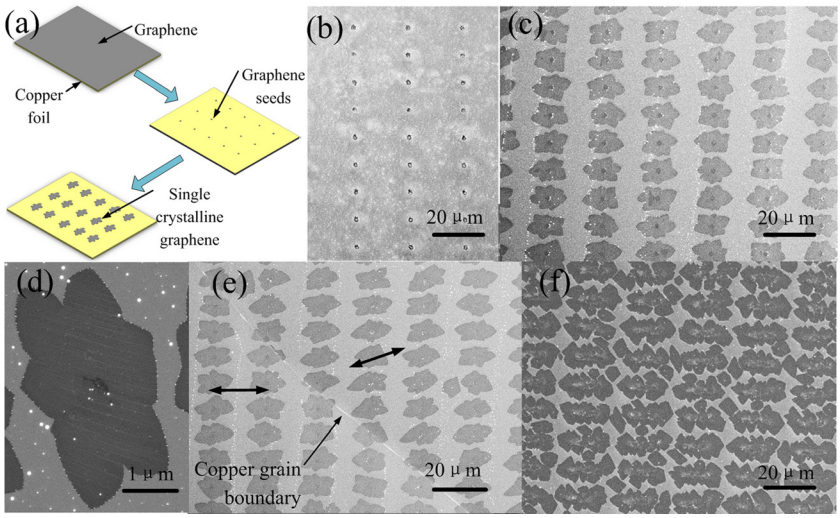

FIG. 1. CVD growth of SCG from controlled nucleation. (a) Schematic view of SCG growth from controlled nucleation. First, grow polycrystalline graphene on copper surface. Next, pattern graphene film into seeds. Then, re-insert copper foil into the furnace to perform re-growth of graphene from artificial seeds. (b) SEM (Scanning electron microscope) image of graphene seeds. (c) SEM image of SCGs grow for 6 min. (d) Zoom in view of a star-like shaped SCG grain. (e) SCGs on two adjacent copper grains. Two arrows show two different orientations of SCGs. (f) SEM image of many tiny "satellite grains" generated around large seeds.

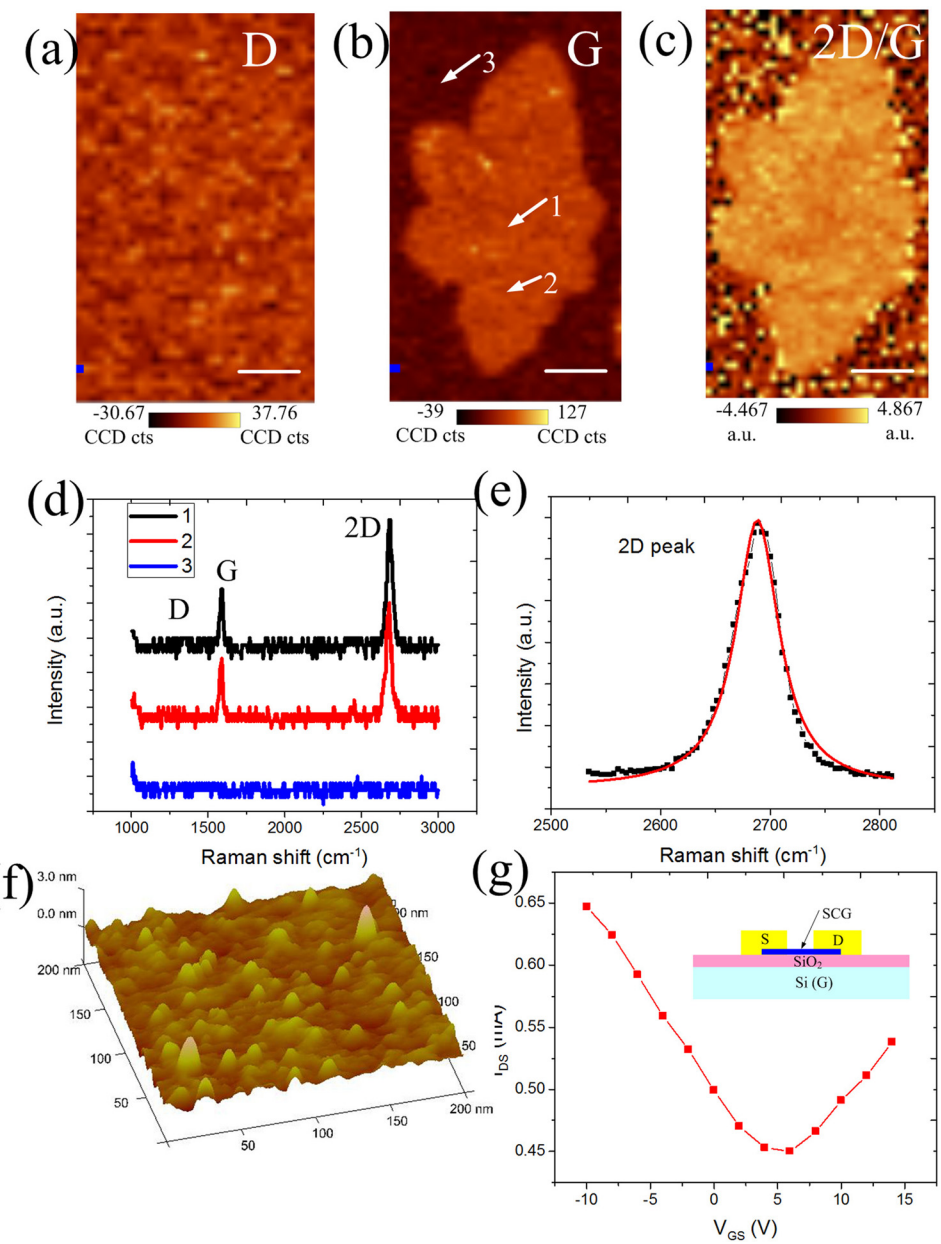

FIG. 2. Characterization of SCG. (a) Raman D peak intensity image of a SCG grain. (b) Raman G peak intensity image of the SCG grain. (c) Raman 2D/G peak intensity ratio image of the same SCG grain. Scale bars, 2 μm. (d) Raman spectra derived from 3 different positions described in b. (e) Raman 2D peak curve (black dots) and Lorentzian fitting for 2D peak (red line). (f) AFM topographic image of monolayer SCG on SiO_2 surface. The roughness of SCG is 223 pm. (g) I_{DS} vs V_{GS} of a SCG FET. The gate can cause either electron or hole conduction with transition point at $V_{GS} \approx 6$ V. The inset is a schematic view of SCG FET.

LPCVD SCG growth from a randomly distributed graphene seed.[34]

The influences of seed on the results are investigated. Since carbon atoms from methane can attach on graphene seed more easily than on copper surface (mainly on defects), in fact, we implant stronger defects (artificial graphene seeds) to overcome the influence of natural defects on copper and prevent randomly distributed grains. If the seed is too small, it is not strong enough to compete with natural defects, many randomly distributed grains will be observed. But if the seed is too large, the growth mechanism will be different. Instead of the growth of seed itself, we observed several tiny "satellite grains" generated around the original seed (Figure 1(f)). In our experiment, the appropriate size of seed is ~0.5–1.5 μm. Small amount of multilayer graphene seeds are inevitable. But mono- other than multilayer SCG is generated from multilayer seeds because of the much lower growth rate of the adlayer. Thus, the thickness of the seed does not affect the results. The quality of seed is extremely important to the results. With prominent defects in the seed, the grains usually show large D peak (defect) in Raman spectrum, and multiple grains instead of one SCG were sometimes observed to grow from a single shared seed. The main reason that our SCG is superior to reported[32] is that we use high quality graphene seeds, and protect them from the copper loss before growth. Orientation is an important feature of CVD graphene grains. Figure 1(e) shows SCGs grown on two adjacent copper grains. Samples on the same copper grains have similar orientation, and distinct orientations of graphene are clearly identified corresponding to different Cu grains and grain orientations. We anticipate that large SCG device arrays with controllable orientation could be realized by controlling the grain orientation of copper foil.

After graphene growth, we performed Raman spectroscopy and mapping on SCG arrays transferred onto SiO_2/Si substrate. The intensities of detected graphene Raman peaks, D (~1350 cm^{-1}), G (~1580 cm^{-1}), and 2D (~2680 cm^{-1})/G ratio were extracted and their distributions (Raman maps) are plotted in Figures 2(a)–2(c) for a single SCG grain. Raman spectra derived from 3 different locations described in Figure 2(b) are shown in Figure 2(d). Spectra 1 and 2 show typical features of monolayer graphene: ~0.5 G to 2D intensity ratio, and a symmetric 2D band centered at ~2680 cm^{-1}. Lorentzian fitting of 2D peak further proofs the monolayer nature of SCG (Figure 2(e)), because 2D peak curve of a monolayer graphene can be fitted by a single Lorentzian peak, while a bi-layer requires four Lorentzians. Good uniformity of the SCG thickness was indicated by 2D/G peak intensity ratio image shown in Figure 2(c). Negligibly small D peak (the intensity ratio of D band to G band is less than 5%) is over most of the area within graphene grain shown in Figure 2(a), indicating very low-defect and single-crystalline nature of our sample, since grain boundary could increase D peak intensity. Spectrum derived from the center (spectrum 1) shows very small D peak (defects), indicating good quality of our seed, while graphene grains reported by Wu *et al.*[32] have prominent defects at the center. AFM (atomic force microscope) topographic image of SCG on SiO_2 surface demonstrates the roughness of 223 pm (Figure 2(f)), close to the roughness of monolayer graphene on SiO_2 measured by Koenig *et al.*[35]

Measuring carrier mobility is another common way to evaluate film quality. SCG field effect transistors (FETs) were fabricated on a silicon substrate with a top gate thermal oxide layer. The I_{DS} versus V_{GS} curve shows electron/hole conduction shifted at a transition point (Dirac point) of $V_{GS} \approx 6$ V (Figure 2(e)). The small shift of Dirac point could be caused by PMMA (polymethyl methacrylate) residue during transfer process.[19] Carrier mobility of graphene can be deduced from[15]

$$\mu = \frac{\Delta I_{DS}}{C_{OX}\frac{W}{L}V_{DS}\Delta V_{GS}}, \quad (1)$$

where L and W are FET length and width, respectively, $C_{OX} = \varepsilon_{OX}\varepsilon_0 t_{OX}$ is gate oxide capacitance ($\varepsilon_{OX} = 3.9$ is silicon dioxide permittivity, ε_0 is vacuum permittivity, and t_{OX} is gate oxide thickness). The carrier mobility of 5500 cm^2 V^{-1} s^{-1} is deduced under ambient conditions. This high carrier mobility is comparable to or even larger than that of SCG from regular CVD growth reported in the literature (~5200 cm^2 V^{-1} s^{-1}, Ref. 36). We believe the carrier mobility of SCG could be even larger by using boron nitride substrates to reduce the charge impurities trapped in SiO_2.[37]

Large-scale free-standing SCG array was realized based on this graphene growth technique. First, SCGs were etched into rectangular beam arrays by O_2 plasma dry etching. The electrode fabrication involves photolithography, Cr/Au electron-beam evaporation, and metal lift-off. BOE (buffered oxidize etcher) was applied to etch SiO_2 beneath SCGs and release the free-standing structures, followed by critical point drying to avoid stiction. This well-organized large-scale free-standing SCG array on Si substrate is shown in Figure 3(a), in which the distance between adjacent SCG beams is identical to the distance between original seeds. Therefore, each beam is corresponding to an individual SCG grain.

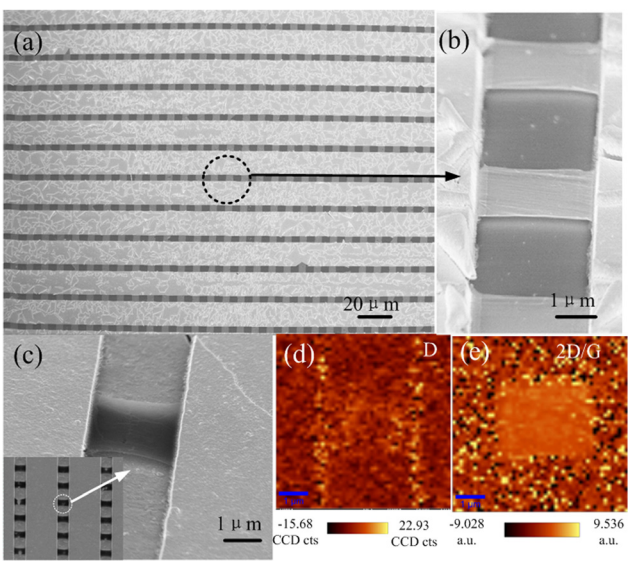

FIG. 3. Large scale suspended SCG beam arrays. (a) SEM image of part of the large scale SCG beam arrays on Si substrate. (b) Zoom in view of the suspended SCG beams. (c) Zoom in view of a suspended SCG beam on flexible PET substrate. The inset shows the SCG arrays on PET substrate. (d) Raman D peak intensity image of a single SCG beam, indicating negligibly small defects on the beam. (e) Raman 2D/G peak intensity ratio image of the same SCG beam, which shows good uniformity of the beam thickness.

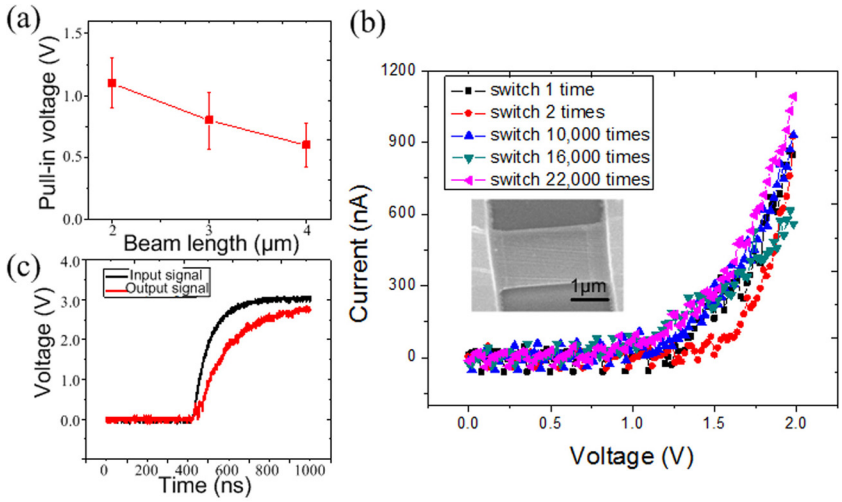

FIG. 4. SCG NEMS switch. (a) Relation between SCG beam length and pull-in voltage. The pull-in voltages of SCG switches tested was around 1 V. Longer beams with smaller spring constant have smaller pull-in voltages. (b) I-V curves of a graphene device switched 1, 2, 10,000, 16,000, and 22,000 times, respectively. (c) Switch speed measurement. The difference between input and output signal is about 100 ns.

Figure 3(d) demonstrates that the beams have small D peak, indicating negligibly small defect. Good uniformity of the graphene beam thickness was indicated by 2D/G peak intensity ratio image shown in Figure 3(e). This technique provides a step-forward practical graphene-based devices. Besides devices on rigid Si substrate, flexible graphene devices are also highly desired for broader applications. So we transferred SCGs on flexible polymer (Poly (ethylene terephthalate) (PET)) substrate and fabricated large-scale suspended SCG beam arrays on it (Figure 3(c)). This device provides a platform for flexible SCG NEMS sensors and actuators.

In order to explore the properties of SCG in NEMS region, the single crystalline graphene NEMS switch is demonstrated. Top SCG film could be pulled to be in contact with the conductive substrate when the applied DC voltage is larger than a threshold value, pull-in voltage, and a sharp increase of the current will be observed; on the contrary, the contact will be broken by an elastic force after the bias is removed. The pull-in voltage is given by

$$V_{pull-in} = \sqrt{\frac{8kg_0^3}{27\varepsilon A}}, \tag{2}$$

where k is the spring constant of the beam, g_0 is the gap between beam and substrate, ε is vacuum permittivity, and A is the size of suspended graphene beam over lower electrodes. From Figure 4(a), the pull-in voltages of our graphene switches tested were around 1 V, which are equal to or smaller than other graphene NEMS switches reported so far.[32,33,38] Longer beams with smaller spring constant have smaller pull-in voltages. Switching speed of our SCG switch was characterized by applying a step signal to the device input terminals, while the output signal was measured concurrently (Figure 4(c)). Delay time between these two signals was only about 100 ns, which indicates an upper bound of the intrinsic switching speed of the switch, while conventional MEMS/NEMS usually have a switching speed in the microsecond regime.

Life time limited by broken failure is the bottleneck of graphene NEMS (resonators[19] and switches[32,33]). We believe mechanically weaker grain boundaries are mainly responsible for it. Polycrystalline graphene switches were observed to degrade and be broken after operating only 4–5 times.[32] Our SCG switches could operate continuously 22 000 times without failure (Figure 4(b)), which life time is two orders longer than that of other graphene NEMS switches reported so far (500 times for mechanically exfoliated graphene NEMS switches[39]). I-V curves in Figure 4(b) show better repeatability than polycrystalline graphene switches,[32] indicating that the SCG switch is very stable and does not degrade after long time operation.

In conclusion, we develop a top-down approach to grow wafer-scale SCG arrays. Site- and alignment-controlled SCG array with superb properties was achieved. Large array of free-standing SCG beams were fabricated. Based on this approach, high quality SCG is introduced into NEMS region, and nano switches with excellent performance (outstanding long lifetime) were fabricated and characterized. This technique not only clearly demonstrates the promise of wafer-size SCG devices with reliable superb performances but also opens a new regime for single crystalline graphene based NEMS.

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