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Min-Woo Jang, Chia-Ling Chen, Walter E. Partlo, Shruti R. Patil, Dongjin Lee, Zhijang Ye, David Lilja, T. Andrew Taton, Tianhong Cui, and Stephen A. Campbell

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A pure single-walled carbon nanotube thin film based three-terminal microelectromechanical switch

Min-Woo Jang,[1] Chia-Ling Chen,[1] Walter E. Partlo III,[2] Shruti R. Patil,[1] Dongjin Lee,[3] Zhijang Ye,[3] David Lilja,[1] T. Andrew Taton,[2] Tianhong Cui,[3] and Stephen A. Campbell[1,a)]
[1]*Department of Electrical and Computer Engineering, University of Minnesota, 200 Union St. SE, Minneapolis, Minnesota 55455, USA*
[2]*Department of Chemistry, University of Minnesota, 207 Pleasant St. SE, Minneapolis, Minnesota 55455, USA*
[3]*Department of Mechanical Engineering, University of Minnesota, 111 Church St. SE, Minneapolis, Minnesota 55455, USA*

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The electrical and physical properties of pure single-walled carbon nanotube thin films deposited through a layer-by-layer-self-assembly process are discussed. The film thickness was proportional to the number of dipping cycles. The film resistivity was estimated as 2.19×10^{-3} Ω cm after thermal treatment processes were performed. The estimated specific contact resistance to gold electrodes was 6.33×10^{-9} Ω m^2 from contact chain measurements. The fabricated three-terminal microelectromechanical switch using these films functioned as a beam for multiple switching cycles with a 4.5 V pull-in voltage. This switch is believed to be a promising device for low power digital logic applications. © *2011 American Institute of Physics*. [doi:10.1063/1.3553227]

Carbon nanotubes (CNTs) have high electrical conductivity, high surface area, and superior chemical and physical stability, which make them promising materials for functional thin films.[1] For microelectromechanical system (MEMS) and nanoelectromechanical system (NEMS) applications, CNTs could provide high frequency and low operation voltage due to its unique physical properties such as low mass density, high stiffness, and high yield strength. Layer-by-layer (LbL) assembly is a simple and adaptable process by which well-controlled CNT thin films can be deposited.[2] Various composite films based on LbL assembly of CNTs with copolymers have recently been reported;[3–5] however, these films are very resistive unless the CNTs are aligned.

In previous work,[6,7] we demonstrated functional 1.6 GHz two-terminal NEMS switches with very low pull-in voltages compared to other reports[8] using the aligned composite single-walled carbon nanotube (AC-SWNT) films by dielectrophoresis process with LbL self-assembly. This performance was made possible by the excellent properties of the AC-SWNT films for this application including their high Young's moduli (350–830 GPa), high yield strengths, and low mass densities,[6] as well as the use of very narrow gaps (~20 nm) for electrostatic actuation. The alignment was necessary because the copolymer used as a positive charged layer for the LbL process, poly(diallyldimethylammonium chloride), is insulating high resistivity films with poor contact reliability. The CNT dielectrophoretic deposition process, however, is not easily adapted to circuit applications because it requires a strong field for each device during the deposition process.

To resolve these issues, we developed an LbL self-assembly process to produce purely carbon nanotube based thin film without copolymers. All CNT films were first introduced by Lee *et al.*[9] using multiwalled nanotubes. We have elected to use SWNTs due to their superior electrical properties.[10,11] We have adopted a succinic acid peroxide[12] (SAP) treatment of the CNTs to produce negative carboxylic acid functional groups on their exterior of the tubes instead of the more commonly used nitric acid oxidation approach.[13] This SAP approach uses radical intermediates to introduce carboxyethyl groups to the double bonds on the SWNT sidewalls. This type of treatment does not damage the SWNT and shorten them to the extent that nitric acid oxidation does,[13] better preserving the desired SWNT electrical and mechanical properties. The copolymer was replaced with a positively charged SWNT by attaching positive NH_3^+ functional groups.[9]

Sufficiently functionalized dispersions were found to be stable for more than 3 months after sonication. LbL self-assembly deposition is done by sequentially dipping the substrate in the two oppositely charged dispersions. To find the optimal dipping time for each dispersion, we performed quartz crystal microbalance measurements using a QCM200 from Stanford Research Systems. In this process a 300 nm thick SiO_2 deposited substrate with gold electrodes was first treated with an O_2 plasma to remove any organic contaminants in an surface technology system (STS) etcher at 100 W of rf power, 100 mTorr pressure, and 100 sccm of oxygen for 5 min, so that its surface is rendered hydrophilic. Next, the substrate was dipped into the positively functionalized SWNT dispersion for 5 min. The substrate was rinsed with Milli-Q water for 2 min and again for 1 min in the different beakers to remove unreacted SWNT debris. Then the substrate was dipped into the negatively functionalized SWNT dispersion for 10 min and the rinse process was repeated. This cycle was repeated until the desired film thickness was reached. On a 4 in. wafer, the standard deviation of thickness was less than 10% of the median thickness. This result reflects the self-limiting nature of the LbL process given that it was achieved in a simple, stagnant, and fully solution-based process. The deposited film thickness is linearly proportional to the total number of deposition cycles at 10 nm per bilayer cycle, as shown in Fig. 1(a). Moreover, as the number of

a)Electronic mail: campb001@umn.edu.

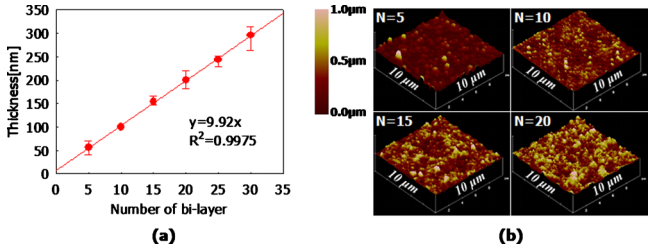

FIG. 1. (Color online) (a) All-SWNT film deposition rate per each bilayer and (b) atomic force microscope scanned images depending on total number of deposit cycles.

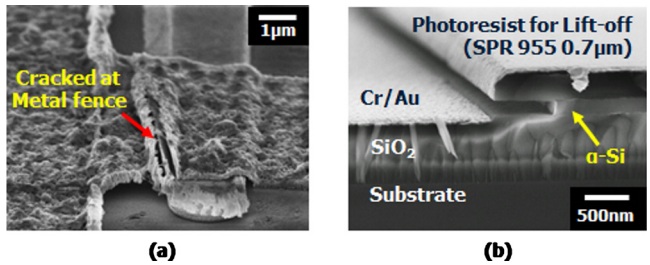

FIG. 3. (Color online) (a) Scanning electron microscope (SEM) image of a cracked film at metal fence in our initial attempts and (b) cross-section SEM image of after metal evaporation showing modified LOR process.

deposition cycles increases, the root-mean-square surface roughness of the film increased at the rate of 1.3 nm per cycle, as shown in Fig. 1(b). This was thought to be due to the increased chance that agglomerates and impurities could be formed when the number of deposit cycles increased.

The electrical properties of 110 nm thick all-SWNT films were characterized by measuring bar resistors and contact chains, as shown in Fig. 2. The width of the measured SWNT film bar resistors is 100 μm and their lengths are 700, 1000, 2200, and 4200 μm, respectively. The resistance was measured at 1.0 V and the resistivity was estimated using the slope of the resistance versus length plot. The extracted resistivity was about 2.9 Ω cm, as shown in Fig. 2(a), which is larger than previous reports which are typically on the order of 10^{-3} Ω cm.[14,15] This may result from the disruption of the conjugated carbon sp^2 orbitals on the SWNT exterior surface with the formation of surface functional groups.[9] To improve the resistivity of the film, thermal treatments were applied. As with the MWNT films of Lee *et al.*,[9] this was very effective in reducing the film resistivity. The first step is to anneal the film at 150 °C for 12 h in vacuum (2–5 mTorr) to form an amide between the –COOH and –amine functional groups. The film resistivity decreased by about two orders of magnitude to 4.92×10^{-2} Ω cm after this anneal. This could be attributed to improved electron flow between adjacent SWNTs that are cross-linked via amide formation.[9] The second anneal was performed at 300 °C in a hydrogen atmosphere for 2 h to remove the residual surface functional groups on the SWNTs.[9] The film resistivity after this anneal was 2.19×10^{-3} Ω cm. This is about four times smaller than that of our previous aligned composite film deposited through copolymer based LbL process.[6] The film thickness after this second anneal was reduced by about 10%. We believe that this is due to shortened average contact distance between coarsely connected SWNT bundles which, in turn, results in a further decrease of the film resistivity.

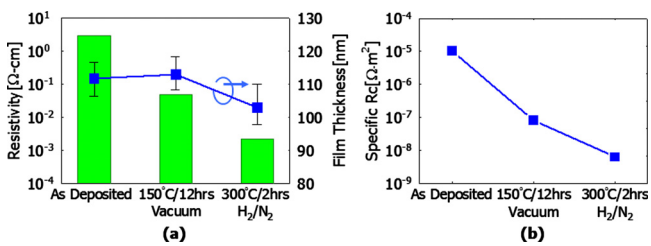

FIG. 2. (Color online) (a) Extracted film resistivity by fitting measured resistances from 100 μm wide bar resistors vs their lengths and (b) extracted specific contact resistance for each thermal treatment.

The specific contact resistance could be estimated by fitting the measured resistances of contact chains.[16] The contact chain test structure has 50 SWNT film islands that are 4 μm wide and 30 μm long. For each island, there are two gold contacts. Therefore, there are 100 contacts with dimensions of 4 μm long and 10 μm wide. The extracted specific contact resistance was 6.33×10^{-9} Ω m^2 in the case of fully annealed films. This is comparable with other reports.[16–18]

We fabricated three-terminal MEMS switches for digital logic applications. In our initial attempts a substrate with 70 nm Au/10 nm Cr electrodes was prepared with a conventional lift-off process. However, this produced high metal fences at the edge of photoresist. Since the cantilever film is essentially conformal, the discontinuous surface topography will lead to an extreme geometry in the SWNT film, creating a stress riser which will lead to premature mechanical failure of the cantilever. We have observed broken SWNT films near the metal fences after several switching events, as shown in Fig. 3(a). To resolve this problem, we developed a metal-fence-free and topographically flat substrate, as shown in Fig. 3(b) and schematically in Fig. 4(a), by adopting an embedded metal process and a modified lift-off resist (LOR) process. 300 nm thick plasma enhanced chemical vapor deposition amorphous silicon (α-Si) was used instead of the

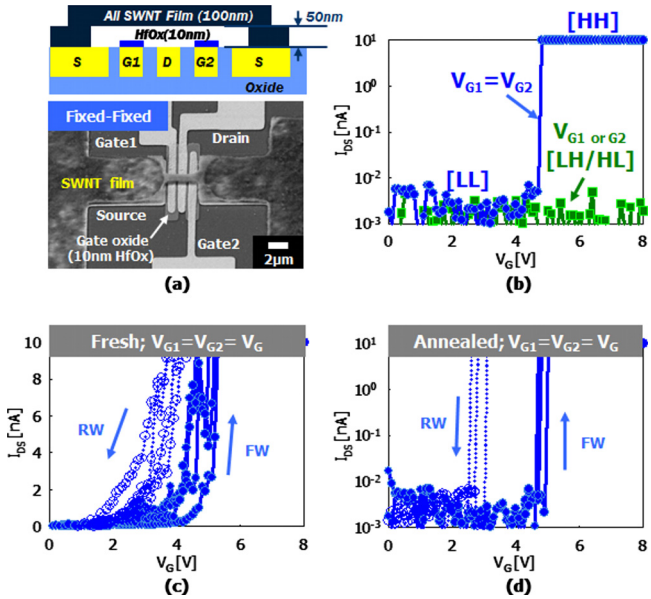

FIG. 4. (Color online) (a) SEM image and schematic of a device under test on the metal fence-free and embedded metal substrate, (b) NAND operation of designed device, (c) I_{DS}-V_G characteristics under repeated switching test of a fresh device, and (d) I_{DS}-V_G characteristics under repeated switching test of a fully annealed device.

LOR since it can be isotropically dry etched in a more controllable manner than the typical wet-developed LOR processes. Prior to metal evaporation, the oxide was etched 100 nm deep to form the embedded metal structure. When the cantilever is activated, it will contact both gate and drain electrodes. To insulate the gate electrodes, we used 10 nm hafnium oxide by atomic layer deposition (ALD), which was patterned by dry etch. The ALD hafnium dioxide was chosen because its thickness is precisely controlled, and the large permittivity of hafnium oxide minimizes any increase in pull-in voltage. To minimize stiction, we used dry etching for device release instead of wet etching. 50 nm thick α-Si was used as a sacrificial layer. The all-SWNT film was deposited and patterned on top of the α-Si, after anchor areas were opened. Finally, to release the beams the α-Si under the patterned SWNT film was removed by dry etching in an STS etcher at 300 W, 300 mTorr, and 200 sccm SF_6 flow for about 15 min. It was found that this etch had no measurable impact on the all-SWNT film.

Figure 4 shows the I-V characteristics of a fabricated device with an all-SWNT film. The measured device uses an all-SWNT film 100 nm thick, 1 μm wide, 3.45 μm long, and α-Si as a sacrificial layer about 50 nm thick. The width and spacing of gate and drain electrodes patterned with an i-line stepper are about 0.75 and 0.3 μm, respectively. This device behaves like a two-input NAND gate, as shown in Fig. 4(b). The freestanding all-SWNT membrane is electrically connected to the drain electrode when both gate inputs are biased higher than 4.2 V (highhigh). In contrast, when only one of two gates was biased and the other was grounded (lowhigh or highlow), or both were held low (lowlow), no current was observed prior to gate oxide breakdown. After a limited number (typically 5–10) of switching events, the device performance becomes quite repeatable. However, the transition from off-state to on-state is not abrupt, as shown in Fig. 4(c). It is believed that upon release some SWNT bundles deflect from the bottom of the film, and so have a reduced air gap. As a result, these discrete whiskers pull in at a lower voltage. This can be resolved by fusing the bundles through the previously described two step thermal treatments prior to release, as shown in Fig. 4(d). The transition is essentially discontinuous in the annealed device, corresponding to zero subthreshold swing. The gap between pull-in and pull-out voltages, hysteresis, is more than 2 V. In the previous work, the hysteresis was negligibly small compared to this result.[7] The primary cause may be due to the different amount of gold diffusion through enhanced silicon solubility of gold during thermal treatments. Therefore, the gold electrode surface would be much rougher than the unannealed α-Si surface.[19] This reduces the pull-in voltage by increasing the total actuating area, but it also may increase stiction. To remove this effect, we could replace gold with some other metal with better stability to α-Si such as Pd or Nb, which may also make better Ohmic contact with SWNT.[20]

In summary, an all-SWNT film was deposited wafer through LbL self-assembly without the use of a copolymer, resulting in 75% reduction of resistivity compared to our previous composite film with copolymer. The deposited film thickness could be well controlled by changing the number of dipping cycles. Moreover, we demonstrated that a three-terminal MEMS switch built with this all-SWNT thin film behaved like a NAND gate. Through thermal treatments, its on- and off-current ratio could be dramatically improved as well as the electrical properties of the all-SWNT film. This three-terminal MEMS switch using the all-SWNT film is believed to be a very promising device for varieties of low power digital logic applications.

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[1] R. H. Baughman, A. A. Zakhidov, and W. A. de Heer, Science **297**, 787 (2002).
[2] G. Decher, Science **277**, 1232 (1997).
[3] M. Michel, A. Taylor, R. Sekol, P. Podsiadlo, P. Ho, N. Kotov, and L. Thompson, Adv. Mater. **19**, 3859 (2007).
[4] M. Zhang, Y. Yan, K. Gong, L. Mao, Z. Guo, and Y. Chen, Langmuir **20**, 8781 (2004).
[5] M. Zhang, L. Su, and L. Mao, Carbon **44**, 276 (2006).
[6] M. Lu, M. W. Jang, S. A. Campbell, and T. Cui, Appl. Phys. Lett. **94**, 261903 (2009).
[7] M. W. Jang, M. Lu, T. Cui, and S. A. Campbell, The 15th International Conference on Solid-State Sensors, Actuators & Microsystems, 2009, pp. 912–915.
[8] G. N. Nielson, M. J. Shaw, O. B. Spahn, G. R. Bogart, M. R. Watts, R. H. Olsson III, P. Resnick, D. Luck, S. Brewer, C. Tigges, and G. Grossetete, Sandia Report No. SAND 2008-0211, 2008.
[9] S. W. Lee, B. S. Kim, S. Chen, S. H. Yang, and P. T. Hammond, J. Am. Chem. Soc. **131**, 671 (2009).
[10] C. Dekker, Phys. Today **52**(May), 22 (1999).
[11] J. W. Mintmire, B. I. Dunlap, and C. T. White, Phys. Rev. Lett. **68**, 631 (1992).
[12] B. Long, T. M. Wu, and F. Stellacci, Chem. Commun. (Cambridge) **2008**, 2788.
[13] J. Liu, A. G. Rinzler, H. Dai, J. H. Hafner, R. K. Bradley, P. J. Boul, A. Lu, T. Iverson, K. Shelimov, C. B. Huffman, F. Rodriguez-Macias, Y.-S. Shon, T. R. Lee, D. T. Colbert, and R. E. Smalley, Science **280**, 1253 (1998).
[14] J. W. Im, I. H. Lee, B. Y. Lee, B. J. Kim, J. Park, W. J. Yu, U. J. Kim, Y. H. Lee, M. J. Seong, E. H. Lee, Y. S. Min, and S. H. Hong, Appl. Phys. Lett. **94**, 053109 (2009).
[15] A. Behnam, L. Noriega, Y. Choi, Z. Wu, A. G. Rinzler, and A. Ural, Appl. Phys. Lett. **89**, 093107 (2006).
[16] S. H. Han, S. H. Lee, J. H. Hur, J. Jang, Y. B. Park, G. Irvin, and P. Drzaic, Solid-State Electron. **54**, 586 (2010).
[17] H. Xu, L. Chen, L. Hu, and N. Zhitenev, Appl. Phys. Lett. **97**, 143116 (2010).
[18] R. Jackson and S. Graham, Appl. Phys. Lett. **94**, 012109 (2009).
[19] B. Ressel, K. C. Prince, and S. Heun, J. Appl. Phys. **93**, 3886 (2003).
[20] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, Nature (London) **424**, 654 (2003).